PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:	Christopher M. Hanna
Application No.:	09/638,245
Filing Date:	14 August 2000
Title:	BTSC ENCODER
Examiner:	Lee, Ping
Art Unit:	2614
Atty. Docket No.:	56233-139 (THAT-3DVCN)
Confirmation No.:	1379

APPEAL BRIEF

Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This Appeal Brief is submitted in support of the Notice of Appeal and Amendment both filed 29 December 2011, wherein Appellant appeals from the rejection in the final Office Action (dated 29 September 2011) of claims 60-93, 106, 109, 110, 112-115, 117, 119, and 134-184 of the subject application. Appellant notes that the final Office Action included a rejection of certain claims (claims 141, 142, 150, and 151) under 35 U.S.C. § 112, second paragraph, for antecedent basis issues, and that the amendment filed 29 December 2011 addressed those rejections. The Advisory Action issued 17 January 2012 indicated that the Amendment would be entered but the 35 U.S.C. § 103 rejections were still deemed proper. The Advisory Action was silent as to the status of the 35 U.S.C. § 112 rejections. As confirmed by the Examiner (via

telephone call with the undersigned on 22 March 2012), the 35 U.S.C. § 112 rejections were overcome by the Amendment filed 29 December 2011.

Real Party In Interest

The subject application is assigned to THAT Corporation, by assignment recorded on 29 July 1997, at Reel 008046, Frame 0250, for U.S. Application No. 08/661,412, now issued as U.S. Patent No. 5,796,842, which is the parent application of U.S. Application No. 09/041,244, now issued as U.S. Patent No. 6,118,879, which is the parent application of the subject application. The noted assignment provides that it applies to all divisional and continuing applications.

Related Appeals and Interferences

To the best of Appellant's and Appellant's representatives' knowledge, there are no related appeals or interferences (see Related Proceedings Appendix).

Status of Claims

1. Claims canceled: 1-59, 94-105, 107, 108, 111, 116, 118, 120-133, 175, and 184
2. Claims withdrawn from consideration, but not canceled: None
3. Claims pending: 60-93, 106, 109, 110, 112-115, 117, 119, 134-174, and 177-183
4. Claims allowed: None
5. Claims rejected: 60-93, 104-106, 109-110, 112-117, 119, 134-174, and 177-183
6. Claims on appeal: 60-93, 106, 109, 110, 112-115, 117, 119, 134-174, and 177-183

Status of Amendments

One amendment has been filed for the subject application subsequent to the final Office Action of 29 September 2011. The appellant filed an amendment under 37 CFR § 1.116 on 29

December 2011. The Examiner indicated by way of the Advisory Action issued 17 January 2012 that the amendment would be entered.

Summary of Claimed Subject Matter

The following is a summary of the claimed subject matter, with supporting references provided relative to the specification of the subject application as filed. The cited references are representative; other support for the claimed subject matter may be present in the application.

A. Summary of Independent Claims

Claim 60

Independent claim 60 of the subject application a system for generating an analog broadcast television stereo signal from a left-channel signal and a right-channel signal, comprising:

Figure 8A and as described on page 35, lines 6-11, "[f]igure 8A shows a block diagram that illustrates one method of using the DSP Embodiment in an analog system. . . . The analog system supplies analog left and right channel audio input signals (shown in Figure 8A as 'L' and 'R', respectively) . . . ."

an analog-to-digital converter arrangement configured so as to convert the right-channel signal to a right digital signal and convert the left-channel signal to a left digital signal;

As shown in Figure 8A, and as described in the paragraph at page 35, lines 8-14, "[t]he analog system supplies analog left and right channel audio input signals (shown in Figure 8A as 'L' and 'R,' respectively) and these signals are applied to the inputs of sixteen bit analog-to-digital converters 810 and 812, respectively. Converters 810, 812 sample their analog input signals using a sampling frequency f_S that is equal to 47,202 Hz (i.e., $3f_H$) and converters 810, 812 thereby generate sequences of sixteen bit digital samples that are representative of the left and right channel audio input signals, respectively."

a signal combiner arrangement coupled to the analog-to-digital converter arrangement and configured so as to generate a summation signal comprising the sum of the

right digital signal and the left digital signal, and generate a difference signal comprising the difference between the right digital signal and the left digital signal;

As described in the paragraph at page 35, lines 14-16, "[t]he signals generated by converters 810 and 812 are applied to encoder 200a where they are received by modules 292 and 294, respectively." The paragraph at page 36, lines 10-12, states, "[i]nput section 210 receives the twenty-four bit words generated by modules 292, 294 and generates therefrom the sum signal that is applied to the sum channel processing section 220 ." The paragraph at page 36, lines 19-21, further states, "[i]nput section 210 also generates the difference signal that is applied to the difference channel processing section 230. As states above, as a result of modules 292, 294, the difference signal may be considered as being attenuated by 24 dB."

a first up-sampler configured to insert additional samples into the summation signal to increase the sample rate of the summation signal;

An interpolator or up-sampler 910 is shown in Figure 9 and described in the specification at page 38, line 23, through page 39, line 2, as follows: "Figure 9 shows a block diagram of one embodiment of composite modulator 822. The latter receives the signals S and D and generates therefrom a digital version of the composite signal. Modulator 822 includes two interpolators 910, 912, two digital low pass filters 914, 916, a digital signal multiplier 918, and two digital signal adders 920, 922. The S and D signals are applied to respective inputs of the interpolators 910 and 912. Interpolators 910, 912, which are alternatively referred to as "up-samplers", interpolate a new sample between every two consecutive samples applied to their inputs, and thereby generate output signals having twice the sampling frequency as the input signals S and D. The output signals generated by interpolators 910 and 912 are applied to respective inputs of low pass filters 914 and 916." An interpolator or up-sampler 910 is also shown in Figure 8D and described at page 41, lines 10-13, as follows, "[p]ortion 822a includes two interpolators 910, 912, two low pass filters 914, 916, digital signal multiplier 918 and a digital signal adder 930. The S signal generated by module 296 is applied to interpolator 910 which 'up-samples' the S signal and applies the up-sampled signal to low pass filter 914."

a second up-sampler configured to insert additional samples into the difference signal to increase the sample rate of the difference signal;

An interpolator or up-sampler 912 is described at page 38, line 23 through page 39, line 2 and shown in Figure 9, as follows: "Figure 9 shows a block diagram of one embodiment of composite modulator 822. The latter receives the signals S and D and generates therefrom a digital version of the composite signal. Modulator 822 includes two interpolators 910, 912, two digital low pass filters 914, 916, a digital signal multiplier 918, and two digital signal adders 920, 922. The S and D signals are applied to respective inputs of the interpolators 910 and 912. Interpolators 910, 912, which are alternatively referred to as "up-samplers", interpolate a new sample between every two consecutive samples applied to their inputs, and thereby generate output signals having twice the sampling frequency as the input signals S and D. The output signals generated by interpolators 910 and 912 are applied to respective inputs of low pass filters 914 and 916. An interpolator or up-sampler 912 is also shown in Figure 8D and described at page 41, lines 10-19, as follows, "[p]ortion 822a includes two interpolators 910, 912, two low pass filters 914, 916, digital signal multiplier 918 and a digital signal adder 930. The S signal generated by module 296 is applied to interpolator 910 which "up-samples" the S signal and applies the up-sampled signal to low pass filter 914. The latter filters this signal and applies the filtered signal to one input terminal of adder 930. A digital pilot tone having twice the normal amplitude (i.e., $2A\cos 2\pi(f_H/f_s)n$) is applied to the other input terminal of adder 930 which generates an output signal by summing the two signals present at its input terminals. The D signal generated by difference channel processing section 230 is applied to interpolator 912 which generates an up-sampled signal that is applied to low pass filter 916."

a sum and difference signal generator arrangement configured so as to generate a first pre-emphasized digital signal as a function of the summation signal, and a second pre-emphasized digital signal as a function of the difference signal;

Sum channel processing section 220 with 75 μs preemphasis filter is shown in Figure 3 and described in the specification at page 16, lines 22-25, "[r]eferring again to Figure 3, the sum channel processing section 220 receives the sum signal and generates therefrom the conditioned sum signal. In particular, the sum signal is applied to a 75 μs preemphasis filter 222." Difference channel processing section 230 with fixed preemphasis filter 232a and fixed preemphasis filter 232b is shown in Figure 3 and described in the specification at page 18, line 16-26, as follows, "[r]eferring again to Figure 3, the difference channel processing section 230

receives the difference signal and generates therefrom the encoded difference signal. The difference signal is applied to a low pass filter 238a which generates therefrom an output signal that is applied to a fixed preemphasis filter 232a. The latter generates an output signal that is applied via line 239 to an input terminal of a wideband compression unit 280, and the encoded difference signal is applied via feedback line 240 to a detector terminal of wideband compression unit 280. The latter generates an output signal that is applied via line 281 to an input terminal of a spectral compression unit 290, and the encoded difference signal is also applied via feedback line 240 to a detector terminal of unit 290. The latter generates an output signal that is applied to a fixed preemphasis filter 232b which in turn generates an output signal that is applied to a clipper 254."

a signal transformation arrangement configured so as to transform the first pre-emphasized digital signal to a digital BTSC compliant L+R signal, and transform the second pre-emphasized digital signal to a digital BTSC compliant L-R signal;

Sum channel processing section 220 is described at page 16, lines 22-23, as follows, "[r]eferring again to Figure 3, the sum channel processing section 220 receives the sum signal and generates therefrom the conditioned sum signal." Difference channel processing section 230 is shown in Figure 3 and described at page 18, lines 16-17, as follows, "[r]eferring again to Figure 3, the difference channel processing section 230 receives the difference signal and generates therefrom the encoded difference signal." Sum channel processing section 220 and difference channel processing section 230 are also shown in Figure 8A.

a digital-to-analog converter arrangement configured to convert the digital BTSC compliant L+R signal to an analog BTSC compliant L+R signal, and the digital BTSC compliant L-R signal to an analog BTSC compliant L-R signal; and

Digital-to-analog converters 814 and 816 are shown Figure 8A and described in the specification on page 36, lines 16-18, and on page 37, lines 5-7, as follows: "The output signal generated by module 296 is applied to a sixteen bit digital-to-analog converter 814 which in turn generates an analog conditioned sum signal." "Referring again to Figure 8A, the output signal generated by filter 238b is applied to a sixteen bit digital-to-analog converter 816 which in turn generates an output signal that is applied to a 6 dB analog amplifier 820."

a composite signal generator arrangement configured so as to generate a composite signal as a function of the combination of the analog BTSC compliant L+R signal and a modulated version of the analog BTSC compliant L-R signal.

Signal adder 940 is shown in Figure 8D and described on page 42, lines 2-4, as follows, "The signals generated by attenuator 936 and amplifier 938 are applied to input terminals of signal adder 940 which sums these signals to generate the analog composite signal."

Claim 63

Independent claim 63 recites a method of generating an analog broadcast television stereo signal from a left-channel signal and a right-channel signal, comprising:

As shown in Figure 8A and described in the specification at page 35, lines 6-7, "[f]igure 8A shows a block diagram that illustrates one method of using the DSP Embodiment in an analog system . . ." and at page 35, lines 8-10, "[t]he analog system supplies analog left and right channel audio input signals (shown in Figure 8A as 'L' and 'R', respectively) . . . ."

converting the right-channel signal to a right digital signal and converting the left-channel signal to a left digital signal;

As shown in Figure 8A and described in the specification at page 35, lines 11-14, "[c]onverters 810, 812 sample their analog input signals using a frequency f_S that is equal to 47,202 Hz (i.e., $3f_H$) and converters 810, 812 thereby generate sequences of sixteen bit digital samples that are representative of the left and right channel audio input signals, respectively."

generating a summation signal comprising the sum of the right digital signal and the left digital signal, and generating a difference signal comprising the difference between the right digital signal and the left digital signal;

As shown in Figure 3, and described on page 15, line 23 through page 16, line 7, "[t]he input section 210 of encoder 200 includes two high pass filters 212, 214, and two signal adders 216, 218. The left channel digital audio input signal L is applied to the input of high pass filter 212, the latter generating therefrom an output signal that is applied to positive input terminals of adders 216, 218. The right channel audio input signal R is applied to the input of high pass filter

214 which generates therefrom an output signal that is applied to a positive input terminal of adder 216 and to a negative input terminal of adder 218. Adder 216 generates a sum signal (indicated in Figure 3 as 'L+R') by summing the output signals generated by filters 212 and 214. Adder 218 generates a difference signal (indicated in Figure 3 as 'L-R') by subtracting the output signal generated by filter 214 from the output signal generated by filter 212. Input section 210 is therefore similar to input section 110 (shown in Figure 1) however, section 210 additionally includes the two high pass filters 212, 214 and generates digital sum and difference signals."

with a first up-sampler, inserting additional samples into the summation signal to increase the sample rate of the summation signal;

As shown in Figure 8A for interpolator 910, and described on page 41, lines 11-13, "[t]he S signal generated by module 296 is applied to interpolator 910 which 'up-samples' the S signal and applies the up-sampled signal to low pass filter 914."

with a second up-sampler, inserting additional samples into the difference signal to increase the sample rate of the difference signal;

As shown in Figure 8D for interpolator 912, and described on page 41, lines 17-19, "[t]he D signal generated by difference channel processing section 230 is applied to interpolator 912 which generates an up-sampled signal that is applied to low pass filter 916."

generating a first pre-emphasized digital signal as a function of the summation signal, and generating a second pre-emphasized digital signal as a function of the difference signal;

As shown in Figure 3 for 75 μs preemphasis filter 222, fixed preemphasis filter 232a, and fixed preemphasis filter 232b and described on page 16, lines 22-27, "[r]eferring again to Figure 3, the sum channel processing section 220 receives the sum signal and generates therefrom the conditioned sum signal. In particular, the sum signal is applied to a 75 μs preemphasis filter 222. The filter 222 in turn generates an output signal that is applied to a static phase equalization filter 228. The filter 228 generates an output signal that is applied to a low pass filter 224 of section 220 which in turn generates the conditioned sum signal." And, again,

at page 18, lines 16-26, "[r]eferring again to Figure 3, the difference channel processing section 230 receives the difference signal and generates therefrom the encoded difference signal. The difference signal is applied to a low pass filter 238a which generates therefrom an output signal that is applied to a fixed preemphasis filter 232a. The latter generates an output signal that is applied via line 239 to an input terminal of a wideband compression unit 280, and the encoded difference signal is applied via feedback line 240 to a detector terminal of wideband compression unit 280. The latter generates an output signal that is applied via line 281 to an input terminal of a spectral compression unit 290, and the encoded difference signal is also applied via feedback line 240 to a detector terminal of unit 290. The latter generates an output signal that is applied to a fixed preemphasis filter 232b which in turn generates an output signal that is applied to a clipper 254."

transforming the first pre-emphasized digital signal to a digital BTSC compliant L+R signal and transforming the second pre-emphasized digital signal to a digital BTSC compliant L-R signal;

Sum channel processing section 220 is shown in Figure 3 and described at page 16, lines 22-23, "[r]eferring again to Figure 3, the sum channel processing section 220 receives the sum signal and generates therefrom the conditioned sum signal." Difference channel processing section 230 is shown in Figure 3 and described at page 18, lines 16-17, "[r]eferring again to Figure 3, the difference channel processing section 230 receives the difference signal and generates therefrom the encoded difference signal." Sum channel processing section 220 and difference channel processing section 230 are also shown in Figure 8A.

converting the digital BTSC compliant L+R signal to an analog BTSC compliant L+R signal, and converting the digital BTSC compliant L-R signal to an analog BTSC compliant L-R signal; and

As shown in Figure 8A, and described for digital-to-analog converter 814 on page 36, lines 16-18, "[t]he output signal generated by module 296 is applied to a sixteen bit digital-to-analog converter 814 which in turn generates an analog conditioned sum signal." And as shown in Figure 8A, and described on page 37, lines 5-7, for digital-to-analog converter 816, "[r]eferring again to Figure 8A, the output signal generated by filter 238b is applied to a sixteen

bit digital-to-analog converter 816 which in turn generates an output signal that is applied to a 6 dB analog amplifier 820."

generating a composite signal as a function of a combination of the analog BTSC compliant L+R signal and a modulated version of the analog BTSC compliant L-R signal.

As shown in Figure 8D and described for signal adder 940 on page 42, lines 2-4, "[t]he signals generated by attenuator 936 and amplifier 938 are applied to input terminals of signal adder 940 which sums these signals to generate the analog composite signal."

Claim 67

Independent claim 67 recites a method of generating an analog broadcast television stereo signal from a left-channel signal and a right-channel signal, comprising:

As shown in Figure 8A and described in the specification at page 35, lines 6-7, "[f]igure 8A shows a block diagram that illustrates one method of using the DSP Embodiment in an analog system . . ." and at page 35, lines 8-10, "[t]he analog system supplies analog left and right channel audio input signals (shown in Figure 8A as 'L' and 'R', respectively) . . . ."

converting the right-channel signal to a right digital signal;

As shown in Figure 8A and described in the specification at page 35, lines 11-14, "[c]onverters 810, 812 sample their analog input signals using a frequency f_S that is equal to 47,202 Hz (i.e., $3f_H$) and converters 810, 812 thereby generate sequences of sixteen bit digital samples that are representative of the left and right channel audio input signals, respectively."

converting the left-channel signal to a left digital signal;

As shown in Figure 8A and described in the specification at page 35, lines 11-14, "[c]onverters 810, 812 sample their analog input signals using a frequency f_S that is equal to 47,202 Hz (i.e., $3f_H$) and converters 810, 812 thereby generate sequences of sixteen bit digital samples that are representative of the left and right channel audio input signals, respectively."

generating a summation signal comprising the sum of the right digital signal and the left digital signal;

As shown in Figure 3, and described on page 16, lines 1-2, "[a]dder 216 generates a sum signal (indicated in Figure 3 as 'L+R') by summing the output signals generated by filters 212 and 214."

generating a difference signal comprising the difference between the right digital signal and the left digital signal;

As shown in Figure 3, and described on page 16, lines 2-4 "[a]dder 218 generates a difference signal (indicated in Figure 3 as 'L-R') by subtracting the output signal generated by filter 214 from the output signal generated by filter 212."

with a first up-sampler, inserting additional samples into the summation signal to increase the sample rate of the summation signal;

As shown in Figure 8A for interpolator 910, and described on page 41, lines 11-13, "[t]he S signal generated by module 296 is applied to interpolator 910 which 'up-samples' the S signal and applies the up-sampled signal to low pass filter 914."

with a second up-sampler, inserting additional samples into the difference signal to increase the sample rate of the difference signal;

As shown in Figure 8D for interpolator 912, and described on page 41, lines 17-19, "[t]he D signal generated by difference channel processing section 230 is applied to interpolator 912 which generates an up-sampled signal that is applied to low pass filter 916."

generating a first pre-emphasized digital signal corresponding to the summation signal;

As shown in Figure 3 for 75 μs preemphasis filter 222, fixed preemphasis filter 232a, and fixed preemphasis filter 232b and described on page 16, lines 22-27, "[r]eferring again to Figure 3, the sum channel processing section 220 receives the sum signal and generates therefrom the conditioned sum signal. In particular, the sum signal is applied to a 75 μs preemphasis filter 222. The filter 222 in turn generates an output signal that is applied to a static phase equalization filter 228. The filter 228 generates an output signal that is applied to a low pass filter 224 of section 220 which in turn generates the conditioned sum signal."

generating a second pre-emphasized digital signal corresponding to the difference signal;

As shown in Figure 3, and at page 18, lines 16-26, "[r]eferring again to Figure 3, the difference channel processing section 230 receives the difference signal and generates therefrom the encoded difference signal. The difference signal is applied to a low pass filter 238a which generates therefrom an output signal that is applied to a fixed preemphasis filter 232a. The latter generates an output signal that is applied via line 239 to an input terminal of a wideband compression unit 280, and the encoded difference signal is applied via feedback line 240 to a detector terminal of wideband compression unit 280. The latter generates an output signal that is applied via line 281 to an input terminal of a spectral compression unit 290, and the encoded difference signal is also applied via feedback line 240 to a detector terminal of unit 290. The latter generates an output signal that is applied to a fixed preemphasis filter 232b which in turn generates an output signal that is applied to a clipper 254."

transforming the first pre-emphasized digital signal to a digital BTSC compliant L+R signal;

Sum channel processing section 220 is described at page 16, lines 22-23, as follows, "[r]eferring again to Figure 3, the sum channel processing section 220 receives the sum signal and generates therefrom the conditioned sum signal."

transforming the second pre-emphasized digital signal to a digital BTSC compliant L-R signal;

Difference channel processing section 230 is shown in Figure 3 and described at page 18, lines 16-17, as follows, "[r]eferring again to Figure 3, the difference channel processing section 230 receives the difference signal and generates therefrom the encoded difference signal." Sum channel processing section 220 and difference channel processing section 230 are also shown in Figure 8A.

converting the digital BTSC compliant L+R signal to an analog BTSC compliant L+R signal;

As shown in Figure 8A, and described on page 36, lines 10-18, for digital-to-analog converter 814, "[i]nput section 210 receives the twenty-four bit words generated by modules 292, 294 and generates therefrom the sum signal that is applied to the sum channel processing section 220. The output signal generated by sum channel processing section 220 is applied to a 'times 16 module' (which may be considered as a 24 dB amplifier) 296. Module 296 thereby compensates for the -24dB attenuators 292, 294 and brings the output of sum channel processing section 220 back to 100% modulation (i.e., back to 'full scale'). The output signal generated by module 296 is applied to a sixteen bit digital-to analog converter 814 which in turn generates an analog conditioned sum signal."

converting the digital BTSC compliant L-R signal to an analog BTSC compliant L-R signal; and

As shown in Figure 8A, and described on page 36, lines 19-20, "[i]nput section 210 also generates the difference signal that is applied to the difference channel processing section 230" and in the same paragraph on page 37, lines 5-7, for digital-to-analog converter 816, "[r]eferring again to Figure 8A, the output signal generated by filter 238b is applied to a sixteen bit digital-to-analog converter 816 which in turn generates an output signal that is applied to a 6 dB analog amplifier 820."

generating a composite signal as a function of a combination of the analog BTSC compliant L+R signal with a modulated version of the analog BTSC compliant L-R signal.

Signal adder 940 is shown in Figure 8D and described on page 42, lines 2-4, as follows, "The signals generated by attenuator 936 and amplifier 938 are applied to input terminals of signal adder 940 which sums these signals to generate the analog composite signal."

Claim 69

Independent claim 69 recites a system for generating an analog broadcast television stereo signal from a left-channel signal and a right-channel signal, comprising:

As shown in Figure 8A and described on page 35, lines 6-11, states, "[f]igure 8A shows a block diagram that illustrates one method of using the DSP Embodiment in an analog

system . . . . The analog system supplies analog left and right channel audio input signals (shown in Figure 8A as 'L' and 'R', respectively) ... ."

an analog-to-digital converter arrangement configured so as to convert the right-channel signal to a right digital signal and convert the left-channel signal to a left digital signal;

As shown in Figure 8A, and as described in the paragraph at page 35, lines 8-14, "[t]he analog system supplies analog left and right channel audio input signals (shown in Figure 8A as 'L' and 'R', respectively) and these signals are applied to the inputs of sixteen bit analog-to-digital converters 810 and 812, respectively. Converters 810, 812 sample their analog input signals using a sampling frequency f_S that is equal to 47,202 Hz (i.e., $3f_H$) and converters 810, 812 thereby generate sequences of sixteen bit digital samples that are representative of the left and right channel audio input signals, respectively."

a signal combiner arrangement coupled to the analog-to-digital converter arrangement and configured so as to generate a summation signal comprising the sum of the right digital signal and the left digital signal, and generate a difference signal comprising the difference between the right digital signal and the left digital signal; wherein the difference between the summation signal and the difference signal, for a given frequency and level, conforms with the difference specified by the BTSC standard;

As described in the paragraph at page 35, lines 14-16, "[t]he signals generated by converters 810 and 812 are applied to encoder 200a where they are received by modules 292 and 294, respectively." The paragraph at page 36, lines 10-12, states, "[i]nput section 210 receives the twenty-four bit words generated by modules 292, 294 and generates therefrom the sum signal that is applied to the sum channel processing section 220 ." The paragraph at page 36, lines 19-21, further states, "[i]nput section 210 also generates the difference signal that is applied to the difference channel processing section 230. As states above, as a result of modules 292, 294, the difference signal may be considered as being attenuated by 24 dB." The paragraph at page 14, lines 17-20, states in part that "[f]igure 3 is a block diagram of one embodiment of a digital BTSC encoder 200 constructed according to the invention. Digital encoder 200 is constructed to provide performance <u>that is functionally equivalent to the performance of idealized encoder 100</u> (shown in Figure 1)" [Emphasis added].

a sum and difference signal generator arrangement configured so as to generate a first pre-emphasized digital signal as a function of the summation signal, and a second pre-emphasized digital signal as a function of the difference signal;

Sum channel processing section 220 with 75 μs preemphasis filter is shown in Figure 3 and described in the specification at page 16, lines 22-25, "[r]eferring again to Figure 3, the sum channel processing section 220 receives the sum signal and generates therefrom the conditioned sum signal. In particular, the sum signal is applied to a 75 μs preemphasis filter 222." Difference channel processing section 230 with fixed preemphasis filter 232a and fixed preemphasis filter 232b is shown in Figure 3 and described in the specification at page 18, line 16-26, as follows, "[r]eferring again to Figure 3, the difference channel processing section 230 receives the difference signal and generates therefrom the encoded difference signal. The difference signal is applied to a low pass filter 238a which generates therefrom an output signal that is applied to a fixed preemphasis filter 232a. The latter generates an output signal that is applied via line 239 to an input terminal of a wideband compression unit 280, and the encoded difference signal is applied via feedback line 240 to a detector terminal of wideband compression unit 280. The latter generates an output signal that is applied via line 281 to an input terminal of a spectral compression unit 290, and the encoded difference signal is also applied via feedback line 240 to a detector terminal of unit 290. The latter generates an output signal that is applied to a fixed preemphasis filter 232b which in turn generates an output signal that is applied to a clipper 254."

a signal transformation arrangement configured so as to transform the first pre-emphasized digital signal to a digital BTSC compliant L+R signal, and transform the second pre-emphasized digital signal to a digital BTSC compliant L-R signal;

Sum channel processing section 220 is described at page 16, lines 22-23, as follows, "[r]eferring again to Figure 3, the sum channel processing section 220 receives the sum signal and generates therefrom the conditioned sum signal." Difference channel processing section 230 is shown in Figure 3 and described at page 18, lines 16-17, as follows, "[r]eferring again to Figure 3, the difference channel processing section 230 receives the difference signal and

generates therefrom the encoded difference signal." Sum channel processing section 220 and difference channel processing section 230 are also shown in Figure 8A.

a composite signal generator arrangement configured so as to generate a digital composite signal as a function of the combination of the digital BTSC compliant L+R signal and a modulated version of the digital BTSC compliant L-R signal; and

As shown in Figure 9, and described on page 38, lines 21-23, "[f]igure 9 shows a block diagram of one embodiment of composite modulator 822. The latter receives the signals S and D and generates therefrom a digital version of the composite signal."

a digital-to-analog converter arrangement configured to convert the digital composite signal to an analog composite signal.

As shown in Figure 8C, and described on page 40, lines 9-11, "[t]his attenuated version of the composite signal is converted to an analog signal by digital-to-analog converter 818 . . . ."

Claim 72

Independent claim 72 recites a method of generating an analog broadcast television stereo signal from a left-channel signal and a right-channel signal, comprising:

As shown in Figure 8A and described in the specification at page 35, lines 6-7, "[f]igure 8A shows a block diagram that illustrates one method of using the DSP Embodiment in an analog system . . ." and at page 35, lines 8-10, "[t]he analog system supplies analog left and right channel audio input signals (shown in Figure 8A as 'L' and 'R', respectively) . . . ."

converting the right-channel signal to a right digital signal and converting the left-channel signal to a left digital signal;

As shown in Figure 8A, and as described in the paragraph at page 35, lines 8-14, "[t]he analog system supplies analog left and right channel audio input signals (shown in Figure 8A as 'L' and 'R,' respectively) and these signals are applied to the inputs of sixteen bit analog-to-digital converters 810 and 812, respectively. Converters 810, 812 sample their analog input

signals using a sampling frequency f_S that is equal to 47,202 Hz (i.e., $3f_H$) and converters 810, 812 thereby generate sequences of sixteen bit digital samples that are representative of the left and right channel audio input signals, respectively."

generating a summation signal comprising the sum of the right digital signal and the left digital signal, and generating a difference signal comprising the difference between the right digital signal and the left digital signal;

As shown in Figure 3, and described on page 16, lines 1-7, "Adder 216 generates a sum signal (indicated in Figure 3 as 'L+R') by summing the output signals generated by filters 212 and 214. Adder 218 generates a difference signal (indicated in Figure 3 as 'L-R') by subtracting the output signal generated by filter 214 from the output signal generated by filter 212. Input section 210 is therefore similar to input section 110 (shown in Figure 1) however, section 210 additionally includes the two high pass filters 212, 214 and generates digital sum and difference signals."

with a first up-sampler, inserting additional samples into the summation signal to increase the sample rate of the summation signal;

As shown in Figure 8A for interpolator 910, and described on page 41, lines 11-13, "[t]he S signal generated by module 296 is applied to interpolator 910 which 'up-samples' the S signal and applies the up-sampled signal to low pass filter 914."

with a second up-sampler, inserting additional samples into the difference signal to increase the sample rate of the difference signal;

As shown in Figure 8D for interpolator 912, and described on page 41, lines 17-19, "[t]he D signal generated by difference channel processing section 230 is applied to interpolator 912 which generates an up-sampled signal that is applied to low pass filter 916."

generating a first pre-emphasized digital signal as a function of the summation signal, and generating a second pre-emphasized digital signal as a function of the difference signal;

As shown in Figure 3 for 75 μs preemphasis filter 222, fixed preemphasis filter 232a, and fixed preemphasis filter 232b and described on page 16, lines 22-27, "[r]eferring again to

Figure 3, the sum channel processing section 220 receives the sum signal and generates therefrom the conditioned sum signal. In particular, the sum signal is applied to a 75 μs preemphasis filter 222. The filter 222 in turn generates an output signal that is applied to a static phase equalization filter 228. The filter 228 generates an output signal that is applied to a low pass filter 224 of section 220 which in turn generates the conditioned sum signal." And, again, at page 18, lines 16-26, "[r]eferring again to Figure 3, the difference channel processing section 230 receives the difference signal and generates therefrom the encoded difference signal. The difference signal is applied to a low pass filter 238a which generates therefrom an output signal that is applied to a fixed preemphasis filter 232a. The latter generates an output signal that is applied via line 239 to an input terminal of a wideband compression unit 280, and the encoded difference signal is applied via feedback line 240 to a detector terminal of wideband compression unit 280. The latter generates an output signal that is applied via line 281 to an input terminal of a spectral compression unit 290, and the encoded difference signal is also applied via feedback line 240 to a detector terminal of unit 290. The latter generates an output signal that is applied to a fixed preemphasis filter 232b which in turn generates an output signal that is applied to a clipper 254."

transforming the first pre-emphasized digital signal to a digital BTSC compliant L+R signal and transforming the second pre-emphasized digital signal to a digital BTSC compliant L-R signal;

Sum channel processing section 220 is shown in Figure 3 and described at page 16, lines 22-23, "[r]eferring again to Figure 3, the sum channel processing section 220 receives the sum signal and generates therefrom the conditioned sum signal." Difference channel processing section 230 is shown in Figure 3 and described at page 18, lines 16-17, "[r]eferring again to Figure 3, the difference channel processing section 230 receives the difference signal and generates therefrom the encoded difference signal." Sum channel processing section 220 and difference channel processing section 230 are also shown in Figure 8A.

generating a digital composite signal as a function of a combination of the digital BTSC compliant L+R signal and a modulated version of the digital BTSC compliant L-R signal; and

As shown in Figure 8B, and described on page 37, lines 21-23, "[f]igure 8B shows a block diagram of one preferred embodiment of a BTSC encoder 200b constructed according to the invention and configured as part of an analog system. Encoder 200b is similar to encoder 200a . . . ." As also described on page 37, line 25 to page 38, line 6, "[t]he output signal generated by module 296 is a scaled version of the conditioned sum signal and is shown in Figure 8B as S. Also, encoder 200b includes a module 298 for amplifying the output signal generated by difference channel processing section 230 by 6 dB (by multiplying by two). The output signal generated by module 298 is a scaled version of the encoded difference signal and is shown in Figure 8B as D. Further, encoder 200b includes a composite modulator 822 for receiving the signals S and D and for generating therefrom a digital version of the composite signal.

converting the digital composite signal to an analog composite signal.

As shown in Figure 8C, and described on page 40, lines 9-11, "[t]his attenuated version of the composite signal is converted to an analog signal by digital-to-analog converter 818 . . . ."

Claim 76

Independent claim 76 recites a method of generating a broadcast television stereo signal from a left-channel signal and a right-channel signal, comprising:

As shown in Figure 8A and described in the specification at page 35, lines 6-7, "[f]igure 8A shows a block diagram that illustrates one method of using the DSP Embodiment in an analog system . . ." and at page 35, lines 8-10, "[t]he analog system supplies analog left and right channel audio input signals (shown in Figure 8A as 'L' and 'R', respectively) . . . ."

converting the right-channel signal to a right digital signal;

As shown in Figure 8A and described in the specification at page 35, lines 11-14, "[c]onverters 810, 812 sample their analog input signals using a frequency f_S that is equal to 47,202 Hz (i.e., $3f_H$) and converters 810, 812 thereby generate sequences of sixteen bit digital samples that are representative of the left and right channel audio input signals, respectively."

converting the left-channel signal to a left digital signal;

As shown in Figure 8A and described in the specification at page 35, lines 11-14, "[c]onverters 810, 812 sample their analog input signals using a frequency f_S that is equal to 47,202 Hz (i.e., $3f_H$) and converters 810, 812 thereby generate sequences of sixteen bit digital samples that are representative of the left and right channel audio input signals, respectively."

generating a summation signal comprising the sum of the right digital signal and the left digital signal;

As shown in Figure 3, and described on page 16, lines 1-2, "[a]dder 216 generates a sum signal (indicated in Figure 3 as 'L+R') by summing the output signals generated by filters 212 and 214."

generating a difference signal comprising the difference between the right digital signal and the left digital signal;

As shown in Figure 3, and described on page 16, lines 2-4 "[a]dder 218 generates a difference signal (indicated in Figure 3 as 'L-R') by subtracting the output signal generated by filter 214 from the output signal generated by filter 212."

with a first up-sampler, inserting additional samples into the summation signal to increase the sample rate of the summation signal;

As shown in Figure 8A for interpolator 910, and described on page 41, lines 11-13, "[t]he S signal generated by module 296 is applied to interpolator 910 which 'up-samples' the S signal and applies the up-sampled signal to low pass filter 914."

with a second up-sampler, inserting additional samples into the difference signal to increase the sample rate of the difference signal;

As shown in Figure 8D for interpolator 912, and described on page 41, lines 17-19, "[t]he D signal generated by difference channel processing section 230 is applied to interpolator 912 which generates an up-sampled signal that is applied to low pass filter 916."

generating a first pre-emphasized digital signal corresponding to the summation signal;

As shown in Figure 3 for 75 μs preemphasis filter 222, fixed preemphasis filter 232a, and fixed preemphasis filter 232b and described on page 16, lines 22-27, "[r]eferring again to Figure 3, the sum channel processing section 220 receives the sum signal and generates therefrom the conditioned sum signal. In particular, the sum signal is applied to a 75 μs preemphasis filter 222. The filter 222 in turn generates an output signal that is applied to a static phase equalization filter 228. The filter 228 generates an output signal that is applied to a low pass filter 224 of section 220 which in turn generates the conditioned sum signal."

generating a second pre-emphasized digital signal corresponding to the difference signal;

As shown in Figure 3, and at page 18, lines 16-26, "[r]eferring again to Figure 3, the difference channel processing section 230 receives the difference signal and generates therefrom the encoded difference signal. The difference signal is applied to a low pass filter 238a which generates therefrom an output signal that is applied to a fixed preemphasis filter 232a. The latter generates an output signal that is applied via line 239 to an input terminal of a wideband compression unit 280, and the encoded difference signal is applied via feedback line 240 to a detector terminal of wideband compression unit 280. The latter generates an output signal that is applied via line 281 to an input terminal of a spectral compression unit 290, and the encoded difference signal is also applied via feedback line 240 to a detector terminal of unit 290. The latter generates an output signal that is applied to a fixed preemphasis filter 232b which in turn generates an output signal that is applied to a clipper 254."

transforming the first pre-emphasized digital signal to a digital BTSC compliant L+R signal;

Sum channel processing section 220 is shown in Figure 3 and described at page 16, lines 22-23, "[r]eferring again to Figure 3, the sum channel processing section 220 receives the sum signal and generates therefrom the conditioned sum signal." As shown in Figure 3 and as described on page 14, lines 17-20, "[f]igure 3 is a block diagram of one embodiment of a digital BTSC encoder 200 constructed according to the invention . . ." and at page 16, lines 1-2, "[a]dder 216 generates a sum signal (indicated in Figure 3 as 'L+R') by summing the output signals generated by filters 212 and 214."

transforming the second pre-emphasized digital signal to a digital BTSC compliant L-R signal;

Figure 3 and as described on page 14, lines 17-20, "[f]igure 3 is a block diagram of one embodiment of a digital BTSC encoder 200 constructed according to the invention . . ." and at page 16, lines 2-4, "[a]dder 218 generates a difference signal (indicated in Figure 3 as 'L-R') by subtracting the output signal generated by filter 214 from the output signal generated by filter 212." Difference channel processing section 230 is shown in Figure 3 and described at page 18, lines 16-17, "[r]eferring again to Figure 3, the difference channel processing section 230 receives the difference signal and generates therefrom the encoded difference signal." Sum channel processing section 220 and difference channel processing section 230 are also shown in Figure 8A.

generating a digital composite signal as a function of a combination of the digital BTSC compliant L+R signal with a modulated version of the digital BTSC compliant L-R signal; and

As shown in Figure 8B, and described on page 37, lines 21-23, "[f]igure 8B shows a block diagram of one preferred embodiment of a BTSC encoder 200b constructed according to the invention and configured as part of an analog system. Encoder 200b is similar to encoder 200a . . . ." As also described on page 37, line 25 to page 38, line 6, "[t]he output signal generated by module 296 is a scaled version of the conditioned sum signal and is shown in Figure 8B as S. Also, encoder 200b includes a module 298 for amplifying the output signal generated by difference channel processing section 230 by 6 dB (by multiplying by two). The output signal generated by module 298 is a scaled version of the encoded difference signal and is shown in Figure 8B as D. Further, encoder 200b includes a composite modulator 822 for receiving the signals S and D and for generating therefrom a digital version of the composite signal.

converting the digital composite signal to an analog composite signal.

As shown in Figure 8C, and described on page 40, lines 9-11, "[t]his attenuated version of the composite signal is converted to an analog signal by digital-to-analog converter 818 . . . ."

Claim 78

Independent claim 78 recites a digital signal processor arrangement for use in generating a broadcast television BTSC encoded stereo signal from a left-channel signal and a right-channel signal, comprising:

As shown in Figure 3, and discussed on page 14, lines 17-23, "[f]igure 3 is a block diagram of one embodiment of a digital BTSC encoder 200 constructed according to the invention. Digital encoder 200 is constructed to provide performance that is functionally equivalent to the performance of idealized encoder 100 (shown in Figure 1). As with idealized encoder 100, digital encoder 200 receives the left and right channel audio input signals and generates therefrom the conditioned sum signal and the encoded difference signal, however, in digital encoder 200 these input and output signals are digitally sampled signals rather than continuous analog signals."

a signal generator arrangement configured so as to generate a digital summation signal as a function of the sum of the left-channel and right-channel signals, and a digital difference signal as a function of the difference between the left-channel and right-channel signals; wherein the difference between the digital summation signal and the digital difference signal, for a given frequency and level, conforms with the difference specified by the BTSC standard;

As shown in Figure 3, and described on page 15, line 23 through page 16, line 7, "[t]he input section 210 of encoder 200 includes two high pass filters 212, 214, and two signal adders 216, 218. The left channel digital audio input signal L is applied to the input of high pass filter 212, the latter generating therefrom an output signal that is applied to positive input terminals of adders 216, 218. The right channel audio input signal R is applied to the input of high pass filter 214 which generates therefrom an output signal that is applied to a positive input terminal of adder 216 and to a negative input terminal of adder 218. Adder 216 generates a sum signal (indicated in Figure 3 as 'L+R') by summing the output signals generated by filters 212 and 214. Adder 218 generates a difference signal (indicated in Figure 3 as 'L-R') by subtracting the output signal generated by filter 214 from the output signal generated by filter 212. Input section

210 is therefore similar to input section 110 (shown in Figure 1) however, section 210 additionally includes the two high pass filters 212, 214 and generates digital sum and difference signals." The paragraph at page 14, lines 17-20, states in part that "[f]igure 3 is a block diagram of one embodiment of a digital BTSC encoder 200 constructed according to the invention. Digital encoder 200 is constructed to provide performance that is functionally equivalent to the performance of idealized encoder 100 (shown in Figure 1)"

a summation signal processing arrangement including a filter arrangement configured to filter the digital summation signal so as to produce a conditioned digital summation signal;

Figure 3 and the paragraph at page 16, lines 22-27, disclose that the sum channel processing section 220 includes a 75 μs preemphasis filter, a static phase equalization filter 228, and a low pass filter 224; further, the paragraph at page 12, lines 17-19, discloses in part "an improved BTSC encoder that includes an input section, a sum channel processing section, and a difference channel processing section all of which are implemented using digital technology".

a difference signal processing arrangement including a pre-emphasis filter arrangement and a signal compressor arrangement, the filter and signal compressor arrangements being configured so as to condition and compress the digital difference signal so as to produce a conditioned digital difference signal;

Figure 3 and the paragraph at page 18, lines 16-26, state "the difference channel processing section 230 receives the difference signal and generates therefrom the encoded difference signal. The difference signal is applied to a low pass filter 238a which generates therefrom an output signal that is applied to a fixed preemphasis filter 232a. The latter generates an output signal that is applied via line 239 to an input terminal of a wideband compression unit 280, and the encoded difference signal is applied via feedback line 240 to a detector terminal of wideband compression unit 280. The latter generates an output signal that is applied via line 281 to an input terminal of a spectral compression unit 290, and the encoded difference signal is also applied via feedback line 240 to a detector terminal of unit 290. The latter generates an output signal that is applied to a fixed preemphasis filter 232b which in turn generates an output signal

that is applied to a clipper 254. Clipper 254 generates an output signal that is applied to a low pass filter 238b which in turn generates the encoded difference signal."

a digital-to-analog converter arrangement for converting the conditioned digital summation signal to an analog sum signal, and the conditioned digital difference signal to an analog difference signal; and

Digital-to-analog converters 814 and 816 are shown Figure 8A and described in the specification on page 36, lines 16-18, and on page 37, lines 5-7, as follows: "The output signal generated by module 296 is applied to a sixteen bit digital-to-analog converter 814 which in turn generates an analog conditioned sum signal." "Referring again to Figure 8A, the output signal generated by filter 238b is applied to a sixteen bit digital-to-analog converter 816 which in turn generates an output signal that is applied to a 6 dB analog amplifier 820.

a signal combiner arrangement configured so as to combine the analog sum signal with a modulated version of the analog difference signal.

As shown in Figure 8D and described for signal adder 940 on page 42, lines 2-4, "[t]he signals generated by attenuator 936 and amplifier 938 are applied to input terminals of signal adder 940 which sums these signals to generate the analog composite signal."

Claim 80

Independent claim 80 recites a digital signal processor arrangement for use in generating a broadcast television BTSC encoded stereo signal from a left-channel signal and a right-channel signal, comprising:

As shown in Figure 3, and discussed on page 14, lines 17-23, "[f]igure 3 is a block diagram of one embodiment of a digital BTSC encoder 200 constructed according to the invention. Digital encoder 200 is constructed to provide performance that is functionally equivalent to the performance of idealized encoder 100 (shown in Figure 1). As with idealized encoder 100, digital encoder 200 receives the left and right channel audio input signals and generates therefrom the conditioned sum signal and the encoded difference signal, however, in

digital encoder 200 these input and output signals are digitally sampled signals rather than continuous analog signals."

a signal generator arrangement configured so as to generate a digital summation signal as a function of the sum of the left-channel and right-channel signals, and a digital difference signal as a function of the difference between the left-channel and right-channel signals; wherein the difference between the digital summation signal and the digital difference signal, for a given frequency and level, conforms with the difference specified by the BTSC standard;

As shown in Figure 3, and described on page 15, line 23 through page 16, line 7, "[t]he input section 210 of encoder 200 includes two high pass filters 212, 214, and two signal adders 216, 218. The left channel digital audio input signal L is applied to the input of high pass filter 212, the latter generating therefrom an output signal that is applied to positive input terminals of adders 216, 218. The right channel audio input signal R is applied to the input of high pass filter 214 which generates therefrom an output signal that is applied to a positive input terminal of adder 216 and to a negative input terminal of adder 218. Adder 216 generates a sum signal (indicated in Figure 3 as 'L+R') by summing the output signals generated by filters 212 and 214. Adder 218 generates a difference signal (indicated in Figure 3 as 'L-R') by subtracting the output signal generated by filter 214 from the output signal generated by filter 212. Input section 210 is therefore similar to input section 110 (shown in Figure 1) however, section 210 additionally includes the two high pass filters 212, 214 and generates digital sum and difference signals." The paragraph at page 14, lines 17-20, states in part that "[f]igure 3 is a block diagram of one embodiment of a digital BTSC encoder 200 constructed according to the invention. Digital encoder 200 is constructed to provide performance that is functionally equivalent to the performance of idealized encoder 100 (shown in Figure 1)"

a summation signal processing arrangement including a filter arrangement configured to filter the digital summation signal so as to produce a conditioned digital summation signal;

Figure 3 and the paragraph at page 16, lines 22-27, disclose that the sum channel processing section 220 includes a 75 μs preemphasis filter, a static phase equalization filter 228,

and a low pass filter 224; further, the paragraph at page 12, lines 17-19, discloses in part "an improved BTSC encoder that includes an input section, a sum channel processing section, and a difference channel processing section all of which are implemented using digital technology".

a difference signal processing arrangement including a pre-emphasis filter arrangement and a signal compressor arrangement, the filter and compressor arrangements being configured so as to condition and compress the digital difference signal so as to produce a conditioned digital difference signal;

Figure 3 and the paragraph at page 18, lines 16-26, state "the difference channel processing section 230 receives the difference signal and generates therefrom the encoded difference signal. The difference signal is applied to a low pass filter 238a which generates therefrom an output signal that is applied to a fixed preemphasis filter 232a. The latter generates an output signal that is applied via line 239 to an input terminal of a wideband compression unit 280, and the encoded difference signal is applied via feedback line 240 to a detector terminal of wideband compression unit 280. The latter generates an output signal that is applied via line 281 to an input terminal of a spectral compression unit 290, and the encoded difference signal is also applied via feedback line 240 to a detector terminal of unit 290. The latter generates an output signal that is applied to a fixed preemphasis filter 232b which in turn generates an output signal that is applied to a clipper 254. Clipper 254 generates an output signal that is applied to a low pass filter 238b which in turn generates the encoded difference signal."

a signal combiner arrangement configured so as to combine the conditioned digital summation signal with a modulated version of the conditioned digital difference signal so as to generate a composite modulated signal; and

Figures 8B and 9 show a composite modulator 822; the paragraph at page 38, lines 2-4, states in part that "encoder 200b includes a composite modulator 822 for receiving the signals S and D and for generating therefrom a digital version of the composite signal"; additionally, the paragraph at page 12, lines 10-12, discloses "a digital BTSC encoder including a composite modulator for generating a composite modulated signal from the conditioned sum signal and the encoded difference signal" [Emphasis added].

a digital-to-analog converter arrangement for converting the composite modulated signal to an analog output signal.

As shown in Figure 8B and described on page 38, lines 4-6, . The digital composite signal generated by modulator 822 is applied to a digital-to-analog converter 818 the output of which is an analog version of the composite signal."

Claim 82

Independent claim 82 recites a method of digitally encoding left and right channel audio signals in accordance with the BTSC standard, comprising:

As shown in Figure 3, and discussed on page 14, lines 17-23, "[f]igure 3 is a block diagram of one embodiment of a digital BTSC encoder 200 constructed according to the invention. Digital encoder 200 is constructed to provide performance that is functionally equivalent to the performance of idealized encoder 100 (shown in Figure 1). As with idealized encoder 100, digital encoder 200 receives the left and right channel audio input signals and generates therefrom the conditioned sum signal and the encoded difference signal, however, in digital encoder 200 these input and output signals are digitally sampled signals rather than continuous analog signals."

providing digital left and digital right channel audio signals;

As shown in Figure 8A and described in the specification at page 35, lines 11-14, "[c]onverters 810, 812 sample their analog input signals using a frequency f_S that is equal to 47,202 Hz (i.e., $3f_H$) and converters 810, 812 thereby generate sequences of sixteen bit digital samples that are representative of the left and right channel audio input signals, respectively."

combining the digital left and digital right channel audio signals to form a digital sum signal and a digital difference signal, wherein the difference between the digital sum signal and the digital difference signal, for a given frequency and level, conforms with the difference specified by the BTSC standard; and

As shown in Figure 3, and described on page 15, line 23 through page 16, line 7, "[t]he input section 210 of encoder 200 includes two high pass filters 212, 214, and two signal adders

216, 218. The left channel digital audio input signal L is applied to the input of high pass filter 212, the latter generating therefrom an output signal that is applied to positive input terminals of adders 216, 218. The right channel audio input signal R is applied to the input of high pass filter 214 which generates therefrom an output signal that is applied to a positive input terminal of adder 216 and to a negative input terminal of adder 218. Adder 216 generates a sum signal (indicated in Figure 3 as 'L+R') by summing the output signals generated by filters 212 and 214. Adder 218 generates a difference signal (indicated in Figure 3 as 'L-R') by subtracting the output signal generated by filter 214 from the output signal generated by filter 212. Input section 210 is therefore similar to input section 110 (shown in Figure 1) however, section 210 additionally includes the two high pass filters 212, 214 and generates digital sum and difference signals." The paragraph at page 14, lines 17-20, states in part that "[f]igure 3 is a block diagram of one embodiment of a digital BTSC encoder 200 constructed according to the invention. Digital encoder 200 is constructed to provide performance that is functionally equivalent to the performance of idealized encoder 100 (shown in Figure 1)"

encoding the digital sum signal and the digital difference signal according to the BTSC standard so as to produce a digital BTSC signal.

As shown in Figure 3 for 75 μs preemphasis filter 222, fixed preemphasis filter 232a, and fixed preemphasis filter 232b and described on page 16, lines 22-27, "[r]eferring again to Figure 3, the sum channel processing section 220 receives the sum signal and generates therefrom the conditioned sum signal. In particular, the sum signal is applied to a 75 μs preemphasis filter 222. The filter 222 in turn generates an output signal that is applied to a static phase equalization filter 228. The filter 228 generates an output signal that is applied to a low pass filter 224 of section 220 which in turn generates the conditioned sum signal." And, again, at page 18, lines 16-26, "[r]eferring again to Figure 3, the difference channel processing section 230 receives the difference signal and generates therefrom the encoded difference signal."

Claim 86

Independent claim 86 recites a digital signal processor for producing a signal encoded according to the BTSC standard, said digital signal processor comprising:

The paragraph at page 30, lines 11-12 and 14-15, discloses that "encoder 200 is preferably implemented using a single digital signal processing chip" and the "DSP Embodiment"; the paragraph at page 35, lines 6-7, describes relative to Figure 8A "one method of using the DSP Embodiment"; the paragraph at page 37, lines 21-23, and page 38, lines 3-4, of the specification describes, in reference to Figure 8B, a "preferred embodiment of a BTSC encoder 200b constructed according to the invention" which is "similar to encoder 200a" and produces a "digital version of the composite signal"; and, Figure 8B depicts encoder 200b.

A) an input section constructed and arranged so as to (1) receive digital left and digital right audio signals and (2) combine the digital left and digital right audio signals so as to form a digital sum signal and a digital difference signal;

The paragraph at page 36, lines 10-11, explains that input section 210 of Figure 8A receives the L and R channels "and generates therefrom the sum signal that is applied to the sum channel processing section"; while the paragraph at page 36, lines 19-20, explains that "[i]nput section 210 also generates the difference signal that is applied to the difference channel processing section 230"; in a similar way, input section 210 of Figure 8B functions as a signal generator arrangement or matrix as it receives L and R signals and generates sum (L+R) and difference (L-R) signals."

B) a difference channel processing section constructed and arranged so as to encode the digital difference signal according to the BTSC standard; and

The paragraph at page 37, line 23, states that encoder 200b is similar to encoder 200a of Figure 8A; Figure 8A shows that an encoded digital difference signal is produced by the difference channel processing section block 230, which is a digital component and equivalent to a digital difference channel section; Figure 8B depicts "a difference channel processing section 230 block. Difference channel processing section 230 is shown in Figure 3 and described at page 18, lines 16-17, as follows, "[r]eferring again to Figure 3, the difference channel processing section 230 receives the difference signal and generates therefrom the encoded difference signal."

C) a sum channel processing section constructed and arranged so as to condition the digital sum signal according to the BTSC standard;

The paragraph at page 37, line 23, states that encoder 200b is similar to encoder 200a of Figure 8A; Figure 8A shows that a conditioned sum signal is produced by the sum channel processing section block 220, which is a digital component and equivalent to a digital sum channel section; Figure 8B depicts "a sum channel processing section 220" block; Figure 3 and the paragraph at page 16, lines 22-27, disclose that the sum channel processing section 220 includes a 75 μs preemphasis filter, a static phase equalization filter 228, and a low pass filter 224; further, the paragraph at page 12, lines 17-19, discloses in part "an improved BTSC encoder that includes an input section, a sum channel processing section, and a difference channel processing section all of which are implemented using digital technology".

D) wherein the difference between the digital sum signal and the digital difference signal, for a given frequency and level, conforms with the difference specified by the BTSC standard.

The paragraph at page 12, lines 17-19, states in part "[t]hese and other objects are provided by an improved BTSC encoder that includes an input section, a sum channel processing section, and a difference channel processing section, all of which are implemented using digital technology"; the paragraph at page 14, lines 18-20, states in part that "[d]igital encoder 200 is constructed to provide performance that is functionally equivalent to the performance of idealized encoder 100 (shown in Figure 1)".

Claim 87

Independent claim 87 recites a system for producing a digital composite modulated BTSC signal comprising a digital BTSC encoder arranged so as to generate a digital BTSC encoded signal, and a digital composite modulator, wherein the digital composite modulator comprises (i) a difference channel processing section constructed and arranged so as to encode a digital difference signal according to the BTSC standard, and (ii) a sum channel processing section constructed and arranged so as to condition a digital sum signal according to the BTSC standard; wherein the BTSC encoder has a frequency response in the digital domain that is substantially equal to the analog frequency response specified by the BTSC standard.

As shown in Figure 8B, and described on page 37, lines 21-22, and page 38, lines 3-4, "one preferred embodiment of a BTSC encoder 200b constructed according to the invention" which produces a "digital version of the composite signal"; Figure 8B depicts the encoder 200b; as described on page 12, lines 17-19, "[t]hese and other objects are provided by an improved BTSC encoder that includes an input section, a sum channel processing section, and a difference channel processing section, all of which are implemented using digital technology"; the paragraph at page 14, lines 18-20, states, in part, that "[d]igital encoder 200 is constructed to provide performance that is functionally equivalent to the performance of idealized encoder 100 (shown in Figure 1)" [Emphasis added]; this statement provides at the very least inherent support for the limitation "wherein the digital BTSC encoder has frequency response in the digital domain that is substantially equal to the analog frequency response specified by the BTSC standard"; as described on page 38, lines 2-4, "encoder 200b includes a composite modulator 822 for receiving the signals S and D and for generating therefrom a digital version of the composite signal"; Figures 8B and 9 show a digital composite modulator 822.

Claim 88

Independent claim 88 recites a method of generating a digital composite modulated BTSC signal, comprising:

As shown in Figure 8B, and described on page 37, lines 21-23, "[f]igure 8B shows a block diagram of one preferred embodiment of a BTSC encoder 200b constructed according to the invention and configured as part of an analog system. Encoder 200b is similar to encoder 200a . . . ."

generating digital left and digital right channel audio signals;

The paragraph at page 35, lines 9-11, of the specification describes, in reference to Figure 8A, "left and right channel audio input signals (shown in Figure 8A as 'L' and 'R,' respectively) and these signals are applied to the inputs of sixteen bit analog-to-digital converters 810 and 812, respectively".

combining said digital left and digital right channel audio signals so as to form a digital sum signal and a digital difference signal;

The paragraph at page 15, line 23 to page 16, line 7, of the specification describes, in reference to Figure 3, "[t]he input section 210 of encoder 200 includes two high pass filters 212, 214, and two signal adders 216, 218. The left channel digital audio input signal L is applied to the input of high pass filter 212, the latter generating therefrom an output signal that is applied to positive input terminals of adders 216, 218. The right channel audio input signal R is applied to the input of high pass filter 214 which generates therefrom an output signal that is applied to a positive input terminal of adder 216 and to a negative input terminal of adder 218. Adder 216 generates a sum signal (indicated in Figure 3 as 'L+R') by summing the output signals generated by filters 212 and 214. Adder 218 generates a difference signal (indicated in Figure 3 as 'L-R') by subtracting the output signal generated by filter 214 from the output signal generated by filter 212".

with a first up-sampler, inserting additional samples into the digital sum signal to increase the sample rate of the digital sum signal;

As shown in Figure 8A for interpolator 910, and described on page 41, lines 11-13, "[t]he S signal generated by module 296 is applied to interpolator 910 which 'up-samples' the S signal and applies the up-sampled signal to low pass filter 914."

with a second up-sampler, inserting additional samples into the digital difference signal to increase the sample rate of the digital difference signal;

As shown in Figure 8D for interpolator 912, and described on page 41, lines 17-19, "[t]he D signal generated by difference channel processing section 230 is applied to interpolator 912 which generates an up-sampled signal that is applied to low pass filter 916."

encoding the digital sum signal and digital difference signal according to the BTSC standard so as to produce a digital BTSC signal; and

As also described on page 37, line 25 to page 38, line 6, "[t]he output signal generated by module 296 is a scaled version of the conditioned sum signal and is shown in Figure 8B as S. Also, encoder 200b includes a module 298 for amplifying the output signal generated by

difference channel processing section 230 by 6 dB (by multiplying by two). The output signal generated by module 298 is a scaled version of the encoded difference signal and is shown in Figure 8B as D.

modulating the digital BTSC signal so as to produce a digital composite modulated BTSC signal.

As shown in Figure 9, and described on page 38, lines 21-23, "[f]igure 9 shows a block diagram of one embodiment of composite modulator 822. The latter receives the signals S and D and generates therefrom a digital version of the composite signal."

Claim 89

Independent claim 89 recites a circuit for encoding digital left and digital right audio signals according to the BTSC standard, comprising:

The paragraph at page 37, lines 21-22, and page 38, lines 3-4, of the specification describes, in reference to Figure 8B, "one preferred embodiment of a BTSC encoder 200b constructed according to the invention" which produces a "digital version of the composite signal"; and Figure 8B depicts the encoder 200b.

a digital matrix unit configured to generate a digital sum channel signal and a digital difference channel signal;

The paragraph at page 37, line 23, states that "encoder 200b is similar to encoder 200a of Figure 8A"; input section 210 of Figure 8B functions as a matrix as it receives L and R signals and produces sum (L+R) and difference (L-R) signals; the Abstract makes this clear: "a matrix means for receiving the digital left and digital right filtered signals, and including means for summing the digital left and digital right filtered signals and thereby generating a digital sum signal, and including means for subtracting one of the digital left and digital right filtered signals from the other of the digital left and digital right filtered signals and thereby generating a digital difference signal."

a sum channel processing unit; and

Figure 8B depicts "a sum channel processing section 220 block."

a difference channel processing unit;

Figure 8B depicts "a difference channel processing section 230 block."

wherein said sum channel processing unit is configured to produce a conditioned digital sum channel signal in response to the digital sum channel signal, and the difference channel processing unit is configured to produce an encoded digital difference channel signal in response to the digital difference channel signal; and wherein the digital matrix has a frequency response in the digital domain that is substantially equal to the analog frequency response specified by the BTSC standard.

Sum channel processing section 220 with 75 μs preemphasis filter is shown in Figure 3 and described in the specification at page 16, lines 22-25, "[r]eferring again to Figure 3, the sum channel processing section 220 receives the sum signal and generates therefrom the conditioned sum signal. In particular, the sum signal is applied to a 75 μs preemphasis filter 222." Difference channel processing section 230 with fixed preemphasis filter 232a and fixed preemphasis filter 232b is shown in Figure 3 and described in the specification at page 18, line 16-26, as follows, "[r]eferring again to Figure 3, the difference channel processing section 230 receives the difference signal and generates therefrom the encoded difference signal. The difference signal is applied to a low pass filter 238a which generates therefrom an output signal that is applied to a fixed preemphasis filter 232a. The latter generates an output signal that is applied via line 239 to an input terminal of a wideband compression unit 280, and the encoded difference signal is applied via feedback line 240 to a detector terminal of wideband compression unit 280. The latter generates an output signal that is applied via line 281 to an input terminal of a spectral compression unit 290, and the encoded difference signal is also applied via feedback line 240 to a detector terminal of unit 290. The latter generates an output signal that is applied to a fixed preemphasis filter 232b which in turn generates an output signal that is applied to a clipper 254"; the paragraph at page 14, lines 18-20, states in part that "[d]igital encoder 200 is constructed to provide performance that is functionally equivalent to the performance of idealized encoder 100 (shown in Figure 1)" [Emphasis added]

Claim 92

Independent claim 92 recites a circuit for producing a digital composite modulated BTSC signal, comprising a matrix unit configured to produce a digital sum signal and a digital difference signal, a digital sum channel processing unit configured to produce a conditioned digital sum signal in response to the digital sum signal, and a digital difference channel processing unit conditioned to produce an encoded digital difference signal in response to the digital difference signal, and a digital modulator unit configured to produce a composite modulated signal in response to the encoded digital difference signal and the conditioned digital sum signal; wherein the matrix unit has a frequency response in the digital domain that is substantially equal to the analog frequency response specified by the BTSC standard.

The paragraph at page 37, line 23, states that encoder 200b is similar to encoder 200a of Figure 8A; input section 210 of Figure 8B functions as a matrix as it receives L and R signals and produces sum (L+R) and difference (L-R) signals; the Abstract recites "a matrix means for receiving the digital left and digital right filtered signals, and including means for summing the digital left and digital right filtered signals and thereby generating a digital sum signal, and including means for subtracting one of the digital left and digital right filtered signals from the other of the digital left and digital right filtered signals and thereby generating a digital difference signal"; the paragraph at page 37, line 23, states that encoder 200b is similar to encoder 200a of Figure 8A; Figure 8A shows that a conditioned sum signal is produced by the sum channel processing section block 220, which is a digital component and equivalent to a sum channel processing unit; Figure 8B depicts "a sum channel processing section 220" block; the paragraph at page 37, line 23, states that encoder 200b is similar to encoder 200a of Figure 8A; Figure 8A shows that an encoded digital difference signal is produced by the difference channel processing section block 230, which is a digital component and equivalent to a difference channel processing unit; Figure 8B depicts "a difference channel processing section 230" block; Figures 8B and 9 show a composite modulator 822; the paragraph at page 38, lines 2-4, states in part that "encoder 200b includes a composite modulator 822 for receiving the signals S and D and for generating therefrom a digital version of the composite signal"; the paragraph at page 14, lines 18-20, states in part that "[d]igital encoder 200 is constructed to provide performance

that is functionally equivalent to the performance of idealized encoder 100 (shown in Figure 1)" [emphasis added].

Claim 106

Independent claim 106 recites a digital signal processor comprising:

As shown in Figure 3, and discussed on page 14, lines 17-23, "[f]igure 3 is a block diagram of one embodiment of a digital BTSC encoder 200 constructed according to the invention. Digital encoder 200 is constructed to provide performance that is functionally equivalent to the performance of idealized encoder 100 (shown in Figure 1)."

(a) an input section configured to receive one or more digital signals and derive therefrom a digital sum signal and digital difference signal;

The paragraph at page 37, line 23, states that encoder 200b is similar to encoder 200a of Figure 8A; the paragraph at page 36, lines 10-11, explains that input section 210 of Figure 8A receives the L and R channels "and generates therefrom the sum signal that is applied to the sum channel processing section"; while the paragraph at page 36, lines 19-20, explains that "[i]nput section 210 also generates the difference signal that is applied to the difference channel processing section 230"; in a similar way, input section 210 of Figure 8B functions as a signal generator arrangement or matrix as it receives L and R signals and generates sum (L+R) and difference (L-R) signals".

(b) a digital difference channel section comprising (i) an adaptive signal weighting system configured to dynamically vary the amplitude and phase of the digital difference signal, and (ii) a multiplier system configured to alter the frequency of the digital difference signal according to the BTSC standard to produce a modified digital difference signal, wherein the adaptive signal weighting system is configured to vary the amplitude of substantially all the spectrum within the digital difference signal responsive to the amplitude of substantially all the spectrum within the digital difference signal;

The paragraph at page 37, line 23, states that encoder 200b is similar to encoder 200a of Figure 8A; Figure 8A shows that an encoded digital difference signal is produced by the

difference channel processing section block 230; Figure 8B depicts "a difference channel processing section 230" block; Figure 3 and the paragraph at page 18, lines 16-26, state "the difference channel processing section 230 receives the difference signal and generates therefrom the encoded difference signal. The difference signal is applied to a low pass filter 238a which generates therefrom an output signal that is applied to a fixed preemphasis filter 232a. The latter generates an output signal that is applied via line 239 to an input terminal of a wideband compression unit 280, and the encoded difference signal is applied via feedback line 240 to a detector terminal of wideband compression unit 280. The latter generates an output signal that is applied via line 281 to an input terminal of a spectral compression unit 290, and the encoded difference signal is also applied via feedback line 240 to a detector terminal of unit 290. The latter generates an output signal that is applied to a fixed preemphasis filter 232b which in turn generates an output signal that is applied to a clipper 254. Clipper 254 generates an output signal that is applied to a low pass filter 238b which in turn generates the encoded difference signal."

(c) a digital sum channel section comprising one or more digital filters for altering the frequency and phase of said digital sum signal according to the BTSC standard to produce a modified digital sum signal; and

As shown in Figure 8B and described on page 37, lines 21-26, "[f]igure 8B shows a block diagram of one preferred embodiment of a BTSC encoder 200b constructed according to the invention and configured as part of an analog system. Encoder 200b is similar to encoder 200a, however, in encoder 200b module 296 amplifies its input signal by 18 dB (by multiplying by 8) rather than by 24 dB as in encoder 200a. The output signal generated by module 296 is a scaled version of the conditioned sum signal and is shown in Figure 8B as S."

(d) an output section for combining said modified digital difference signal and modified digital sum signal to form one or more digital output signals.

As shown in Figure 8B and described on page 37, lines 26 through page 38, line 2, "[a]lso, encoder 200b includes a module 298 for amplifying the output signal generated by difference channel processing section 230 by 6 dB (by multiplying by two). The output signal

generated by module 298 is a scaled version of the encoded difference signal and is shown in Figure 8B as D."

Claim 109

Independent claim 109 recites a digital signal processor comprising:

As shown in Figure 3, and discussed on page 14, lines 17-20, "[f]igure 3 is a block diagram of one embodiment of a digital BTSC encoder 200 constructed according to the invention. Digital encoder 200 is constructed to provide performance that is functionally equivalent to the performance of idealized encoder 100 (shown in Figure 1)."

a) an input section configured to receive one or more digital input signals;

The paragraph at page 37, line 23, states that encoder 200b is similar to encoder 200a of Figure 8A; the paragraph at page 36, lines 10-11, explains that input section 210 of Figure 8A receives the L and R channels "and generates therefrom the sum signal that is applied to the sum channel processing section"; while the paragraph at page 36, lines 19-20, explains that "[i]nput section 210 also generates the difference signal that is applied to the difference channel processing section 230."

b) a sum-channel processing section for creating and conditioning a sum-channel signal according to the BTSC standard from the digital input signals

The paragraph at page 37, line 23, states that encoder 200b is similar to encoder 200a of Figure 8A; Figure 8A shows that a conditioned sum signal is produced by the sum channel processing section block 220, which is a digital component and equivalent to a digital sum channel section; Figure 8B depicts "a sum channel processing section 220" block; Figure 3 and the paragraph at page 16, lines 22-27, disclose that the sum channel processing section 220 includes a 75 μs preemphasis filter, a static phase equalization filter 228, and a low pass filter 224; further, the paragraph at page 12, lines 17-19, discloses in part "an improved BTSC encoder that includes an input section, a sum channel processing section, and a difference channel processing section all of which are implemented using digital technology."

c) a difference-channel processing section for creating and filtering a difference-channel signal according to the BTSC standard from said digital input signals; and

The paragraph at page 37, line 23, states that encoder 200b is similar to encoder 200a of Figure 8A; Figure 8A shows that an encoded digital difference signal is produced by the difference channel processing section block 230; Figure 8B depicts "a difference channel processing section 230" block; Figure 3 and the paragraph from page 18, line 16 to page 19, line 2, disclose that the difference channel processing section 230 includes a low pass filter 238a, a fixed preemphasis filter 232a, a wideband compression unit 280, spectral compression unit 290, fixed preemphasis filter 232b, clipper 254, and low pass filter 238b; further, the paragraph at page 12, lines 17-19, discloses in part "an improved BTSC encoder that includes an input section, a sum channel processing section, and a difference channel processing section all of which are implemented using digital technology."

d) a combining section for transforming the sum-channel signal and the difference-channel signal into one or more output signals according to the BTSC standard;

Figure 8B, the paragraph at page 38, lines 2-4, states in part "encoder 200b includes a composite modulator 822 for receiving the signals S and D and for generating therefrom a digital version of the composite signal". As shown in Figure 8C, and described on page 40, lines 9-11, "[t]his attenuated version of the composite signal is converted to an analog signal by digital-to-analog converter 818 . . . ."

wherein the digital signal processor has a frequency response in the digital domain that is substantially equal to the analog frequency response specified by the BTSC standard.

The paragraph at page 14, lines 18-20, states in part that "[d]igital encoder 200 is constructed to provide performance <u>that is functionally equivalent to the performance of idealized encoder 100</u> (shown in Figure 1)"

<u>Claim 110</u>

Independent claim 110 recites a method of generating one or more digital output signals according to the BTSC standard, comprising:

As shown in Figure 3 and described on page 14, lines 17-18, "Figure 3 is a block diagram of one embodiment of a digital BTSC encoder 200 constructed according to the invention"; the paragraph at page 35, lines 7-8, of the specification describes, in reference to Figure 8A, "[f]igure 8A shows a block diagram that illustrates one method of using the DSP embodiment . . . ."

filtering a digital signal including sum-channel information so as to create a digital sum-channel signal according to the BTSC standard;

Figure 3 shows a sum channel processing section 220 for a digital encoder according to the invention. See the paragraph from page 14, line 17, to page 15, line 6. Sum channel processing section 220 includes three filters in Figure 3: a 75 μs preemphasis filter 222, a static phase equalization filter 228, and a low pass filter 224; Figure 8A shows that a conditioned sum signal is produced by the sum channel processing section block 220; Figure 8A shows a DSP digital encoder 200 of Figure 3 in an integrated circuit implementation; the paragraph at page 14, lines 17-20, states in part that "[f]igure 3 is a block diagram of one embodiment of a digital BTSC encoder 200 constructed according to the invention. Digital encoder 200 is constructed to provide performance that is functionally equivalent to the performance of idealized encoder 100 (shown in Figure 1)" [Emphasis added].

filtering a digital signal including difference-channel information so as to create a digital difference-channel signal according to the BTSC standard; and

Encoder 200 of Figure 3 includes a difference channel processing unit that includes seven filter blocks: low pass filter 238a, fixed preemphasis filter 232a, wideband compression unit 280, spectral compression unit 290, fixed preemphasis filter 232b, clipper 254, and low pass filter 238b; the paragraph at page 12, lines 17-19, states in part "[t]hese and other objects are provided by an improved BTSC encoder that includes an input section, a sum channel processing section, and a difference channel processing section, all of which are implemented using digital technology. Digital encoder 200 is constructed to provide performance that is functionally equivalent to the performance of idealized encoder 100 (shown in Figure 1)" [Emphasis added].

combining the sum-channel signal and the difference-channel signal so as to form one or more digital output signals according to the BTSC standard, wherein the difference

between the sum-channel signal and the difference-channel signal, for a given frequency and level, conforms with the difference specified by the BTSC standard.

Figures 8B-8C and 9 show that the digital sum-channel signal and the digital difference channel signal are combined to form one or more digital output signals; in reference to Figure 8B, the paragraph at page 38, lines 2-4, states in part "encoder 200b includes a composite modulator 822 for receiving the signals S and D and for generating therefrom a digital version of the composite signal"; in reference to Figure 8C, the paragraph at page 40, lines 8-9, states in part "[c]omposite modulator 822 therefore generates from these signals a version of the composite signal"; in reference to Figure 9, the paragraph at page 39, lines 14-15, states in part ". . . signal adder 922 which generates the digital composite signal by summing the two signals present at its inputs"; the paragraph at page 14, lines 17-20, states in part that "[f]igure 3 is a block diagram of one embodiment of a digital BTSC encoder 200 constructed according to the invention. Digital encoder 200 is constructed to provide performance that is functionally equivalent to the performance of idealized encoder 100 (shown in Figure 1)" [Emphasis added].

Claim 112

Independent claim 112 recites a system for generating a broadcast television stereo signal from a left-channel signal and a right-channel signal, comprising:

As shown in Figure 8A and as described on page 35, lines 6-11, "[f]igure 8A shows a block diagram that illustrates one method of using the DSP Embodiment in an analog system. . . . The analog system supplies analog left and right channel audio input signals (shown in Figure 8A as 'L' and 'R', respectively) . . . ."

a signal combiner arrangement configured so as to generate a summation signal comprising the sum of a right digital signal and a left digital signal, and generate a difference signal comprising the difference between the right digital signal and the left digital signal;

As described in the paragraph at page 35, lines 14-16, "[t]he signals generated by converters 810 and 812 are applied to encoder 200a where they are received by modules 292 and 294, respectively." The paragraph at page 36, lines 10-12, states, "[i]nput section 210

receives the twenty-four bit words generated by modules 292, 294 and generates therefrom the sum signal that is applied to the sum channel processing section 220 ." The paragraph at page 36, lines 19-21, further states, "[i]nput section 210 also generates the difference signal that is applied to the difference channel processing section 230. As states above, as a result of modules 292, 294, the difference signal may be considered as being attenuated by 24 dB."

a sum and difference signal generator arrangement configured so as to generate a first pre-emphasized digital signal as a function of the summation signal, and a second pre-emphasized digital signal as a function of the difference signal;

Sum channel processing section 220 with 75 μs preemphasis filter is shown in Figure 3 and described in the specification at page 16, lines 22-25, "[r]eferring again to Figure 3, the sum channel processing section 220 receives the sum signal and generates therefrom the conditioned sum signal. In particular, the sum signal is applied to a 75 μs preemphasis filter 222." Difference channel processing section 230 with fixed preemphasis filter 232a and fixed preemphasis filter 232b is shown in Figure 3 and described in the specification at page 18, line 16-26, as follows, "[r]eferring again to Figure 3, the difference channel processing section 230 receives the difference signal and generates therefrom the encoded difference signal. The difference signal is applied to a low pass filter 238a which generates therefrom an output signal that is applied to a fixed preemphasis filter 232a. The latter generates an output signal that is applied via line 239 to an input terminal of a wideband compression unit 280, and the encoded difference signal is applied via feedback line 240 to a detector terminal of wideband compression unit 280. The latter generates an output signal that is applied via line 281 to an input terminal of a spectral compression unit 290, and the encoded difference signal is also applied via feedback line 240 to a detector terminal of unit 290. The latter generates an output signal that is applied to a fixed preemphasis filter 232b which in turn generates an output signal that is applied to a clipper 254."

a signal transformation arrangement configured so as to transform the first pre-emphasized digital signal to a digital BTSC compliant L+R signal, and transform the second pre-emphasized digital signal to a digital BTSC compliant L-R signal, wherein the difference

between the digital BTSC compliant L+R signal and the digital BTSC compliant L-R signal, for a given frequency and level, conforms with the difference specified by the BTSC standard; and

Sum channel processing section 220 is described at page 16, lines 22-23, as follows, "[r]eferring again to Figure 3, the sum channel processing section 220 receives the sum signal and generates therefrom the conditioned sum signal." Difference channel processing section 230 is shown in Figure 3 and described at page 18, lines 16-17, as follows, "[r]eferring again to Figure 3, the difference channel processing section 230 receives the difference signal and generates therefrom the encoded difference signal." Sum channel processing section 220 and difference channel processing section 230 are also shown in Figure 8A. The paragraph at page 14, lines 17-20, states in part that "[f]igure 3 is a block diagram of one embodiment of a digital BTSC encoder 200 constructed according to the invention. Digital encoder 200 is constructed to provide performance that is functionally equivalent to the performance of idealized encoder 100 (shown in Figure 1)" [Emphasis added].

a composite signal generator arrangement configured so as to generate a digital composite signal as a function of the combination of the digital BTSC compliant L+R signal and a modulated version of the digital BTSC compliant L-R signal.

Figures 8B-8C and 9 show that the digital sum-channel signal and the digital difference channel signal are combined to form one or more digital output signals; in reference to Figure 8B, the paragraph at page 38, lines 2-4, states in part "encoder 200b includes a composite modulator 822 for receiving the signals S and D and for generating therefrom a digital version of the composite signal"; in reference to Figure 8C, the paragraph at page 40, lines 8-9, states in part "[c]omposite modulator 822 therefore generates from these signals a version of the composite signal".

Claim 113

Independent claim 113 recites a method of generating a broadcast television stereo signal from a left-channel signal and a right-channel signal, comprising:

As shown in Figure 8A and described in the specification at page 35, lines 6-7, "[f]igure 8A shows a block diagram that illustrates one method of using the DSP Embodiment in an analog system . . ." and at page 35, lines 8-10, "[t]he analog system supplies analog left and right channel audio input signals (shown in Figure 8A as 'L' and 'R', respectively) . . . ."

generating a summation signal comprising the sum of a right digital signal and a left digital signal, and generating a difference signal comprising the difference between the right digital signal and the left digital signal;

As shown in Figure 3, and described on page 15, line 23 through page 16, line 7, "[t]he input section 210 of encoder 200 includes two high pass filters 212, 214, and two signal adders 216, 218. The left channel digital audio input signal L is applied to the input of high pass filter 212, the latter generating therefrom an output signal that is applied to positive input terminals of adders 216, 218. The right channel audio input signal R is applied to the input of high pass filter 214 which generates therefrom an output signal that is applied to a positive input terminal of adder 216 and to a negative input terminal of adder 218. Adder 216 generates a sum signal (indicated in Figure 3 as 'L+R') by summing the output signals generated by filters 212 and 214. Adder 218 generates a difference signal (indicated in Figure 3 as 'L-R') by subtracting the output signal generated by filter 214 from the output signal generated by filter 212. Input section 210 is therefore similar to input section 110 (shown in Figure 1) however, section 210 additionally includes the two high pass filters 212, 214 and generates digital sum and difference signals."

generating a first pre-emphasized digital signal as a function of the summation signal, and generating a second pre-emphasized digital signal as a function of the difference signal;

As shown in Figure 3 for 75 μs preemphasis filter 222, fixed preemphasis filter 232a, and fixed preemphasis filter 232b and described on page 16, lines 22-27, "[r]eferring again to Figure 3, the sum channel processing section 220 receives the sum signal and generates therefrom the conditioned sum signal. In particular, the sum signal is applied to a 75 μs preemphasis filter 222. The filter 222 in turn generates an output signal that is applied to a static phase equalization filter 228. The filter 228 generates an output signal that is applied to a low

pass filter 224 of section 220 which in turn generates the conditioned sum signal." And, again, at page 18, lines 16-26, "[r]eferring again to Figure 3, the difference channel processing section 230 receives the difference signal and generates therefrom the encoded difference signal. The difference signal is applied to a low pass filter 238a which generates therefrom an output signal that is applied to a fixed preemphasis filter 232a. The latter generates an output signal that is applied via line 239 to an input terminal of a wideband compression unit 280, and the encoded difference signal is applied via feedback line 240 to a detector terminal of wideband compression unit 280. The latter generates an output signal that is applied via line 281 to an input terminal of a spectral compression unit 290, and the encoded difference signal is also applied via feedback line 240 to a detector terminal of unit 290. The latter generates an output signal that is applied to a fixed preemphasis filter 232b which in turn generates an output signal that is applied to a clipper 254."

transforming the first pre-emphasized digital signal to a digital BTSC compliant L+R signal and transforming the second pre-emphasized digital signal to a digital BTSC compliant L-R signal, wherein the difference between the digital BTSC compliant L+R signal and the digital BTSC compliant L-R signal, for a given frequency and level, conforms with the difference specified by the BTSC standard; and

Sum channel processing section 220 is shown in Figure 3 and described at page 16, lines 22-23, "[r]eferring again to Figure 3, the sum channel processing section 220 receives the sum signal and generates therefrom the conditioned sum signal." Difference channel processing section 230 is shown in Figure 3 and described at page 18, lines 16-17, "[r]eferring again to Figure 3, the difference channel processing section 230 receives the difference signal and generates therefrom the encoded difference signal." Sum channel processing section 220 and difference channel processing section 230 are also shown in Figure 8A. The paragraph at page 14, lines 17-20, states in part that "[f]igure 3 is a block diagram of one embodiment of a digital BTSC encoder 200 constructed according to the invention. Digital encoder 200 is constructed to provide performance that is functionally equivalent to the performance of idealized encoder 100 (shown in Figure 1)" [Emphasis added].

generating a digital composite signal as a function of a combination of the digital BTSC compliant L+R signal and a modulated version of the digital BTSC compliant L-R signal.

As shown in Figure 9, and described on page 38, lines 21-23, "[f]igure 9 shows a block diagram of one embodiment of composite modulator 822. The latter receives the signals S and D and generates therefrom a digital version of the composite signal."

Claim 114

Independent claim 114 recites a system for generating a broadcast television stereo signal from a left digital signal and a right digital signal, comprising:

As shown in Figure 8A and described in the specification at page 35, lines 6-7, "[f]igure 8A shows a block diagram that illustrates one method of using the DSP Embodiment in an analog system . . ." and at page 35, lines 8-10, "[t]he analog system supplies analog left and right channel audio input signals (shown in Figure 8A as 'L' and 'R', respectively) . . . ."

(a) circuitry that generates a summation signal comprising the sum of the right digital signal and the left digital signal, and a difference signal comprising the difference between the right digital signal and the left digital signal;

As shown in Figure 3, and described on page 15, line 23 through page 16, line 7, "[t]he input section 210 of encoder 200 includes two high pass filters 212, 214, and two signal adders 216, 218. The left channel digital audio input signal L is applied to the input of high pass filter 212, the latter generating therefrom an output signal that is applied to positive input terminals of adders 216, 218. The right channel audio input signal R is applied to the input of high pass filter 214 which generates therefrom an output signal that is applied to a positive input terminal of adder 216 and to a negative input terminal of adder 218. Adder 216 generates a sum signal (indicated in Figure 3 as 'L+R') by summing the output signals generated by filters 212 and 214. Adder 218 generates a difference signal (indicated in Figure 3 as 'L-R') by subtracting the output signal generated by filter 214 from the output signal generated by filter 212. Input section 210 is therefore similar to input section 110 (shown in Figure 1) however, section 210

additionally includes the two high pass filters 212, 214 and generates digital sum and difference signals."

(b) preemphasis circuitry that generates a first digitally pre-emphasized signal corresponding to the summation signal, and a second digitally pre-emphasized signal corresponding to the difference signal; and

Sum channel processing section 220 with 75 μs preemphasis filter is shown in Figure 3 and described in the specification at page 16, lines 22-25, "[r]eferring again to Figure 3, the sum channel processing section 220 receives the sum signal and generates therefrom the conditioned sum signal. In particular, the sum signal is applied to a 75 μs preemphasis filter 222." Difference channel processing section 230 with fixed preemphasis filter 232a and fixed preemphasis filter 232b is shown in Figure 3 and described in the specification at page 18, line 16-26, as follows, "[r]eferring again to Figure 3, the difference channel processing section 230 receives the difference signal and generates therefrom the encoded difference signal. The difference signal is applied to a low pass filter 238a which generates therefrom an output signal that is applied to a fixed preemphasis filter 232a. The latter generates an output signal that is applied via line 239 to an input terminal of a wideband compression unit 280, and the encoded difference signal is applied via feedback line 240 to a detector terminal of wideband compression unit 280. The latter generates an output signal that is applied via line 281 to an input terminal of a spectral compression unit 290, and the encoded difference signal is also applied via feedback line 240 to a detector terminal of unit 290. The latter generates an output signal that is applied to a fixed preemphasis filter 232b which in turn generates an output signal that is applied to a clipper 254."

(c) transforming circuitry that transforms the first pre-emphasized signal to a digital BTSC L+R signal and that transforms the pre-emphasized second signal to a digital BTSC L-R signal; wherein the difference between the digital BTSC L+R signal and the digital BTSC L-R signal, for a given frequency and level, conforms with the difference specified by the BTSC standard.

Sum channel processing section 220 is described at page 16, lines 22-23, as follows, "[r]eferring again to Figure 3, the sum channel processing section 220 receives the sum signal

and generates therefrom the conditioned sum signal." Difference channel processing section 230 is shown in Figure 3 and described at page 18, lines 16-17, as follows, "[r]eferring again to Figure 3, the difference channel processing section 230 receives the difference signal and generates therefrom the encoded difference signal." Sum channel processing section 220 and difference channel processing section 230 are also shown in Figure 8A.

Claim 134

Independent claim 134 recites system for generating a broadcast television stereo signal from a left-channel signal and a right-channel signal, comprising:

Figure 8A and as described on page 35, lines 6-11, "[f]igure 8A shows a block diagram that illustrates one method of using the DSP Embodiment in an analog system. . . . The analog system supplies analog left and right channel audio input signals (shown in Figure 8A as 'L' and 'R', respectively) . . . ."

an analog-to-digital converter arrangement configured so as to convert the right-channel signal to a right digital signal and convert the left-channel signal to a left digital signal;

As shown in Figure 8A, and as described in the paragraph at page 35, lines 8-14, "[t]he analog system supplies analog left and right channel audio input signals (shown in Figure 8A as 'L' and 'R,' respectively) and these signals are applied to the inputs of sixteen bit analog-to-digital converters 810 and 812, respectively. Converters 810, 812 sample their analog input signals using a sampling frequency f_S that is equal to 47,202 Hz (i.e., $3f_H$) and converters 810, 812 thereby generate sequences of sixteen bit digital samples that are representative of the left and right channel audio input signals, respectively."

a signal combiner arrangement coupled to the analog-to-digital converter arrangement and configured so as to generate a summation signal comprising the sum of the right digital signal and the left digital signal, and generate a difference signal comprising the difference between the right digital signal and the left digital signal;

As shown in Figure 3, and described on page 15, line 23 through page 16, line 7, "[t]he input section 210 of encoder 200 includes two high pass filters 212, 214, and two signal adders

216, 218. The left channel digital audio input signal L is applied to the input of high pass filter 212, the latter generating therefrom an output signal that is applied to positive input terminals of adders 216, 218. The right channel audio input signal R is applied to the input of high pass filter 214 which generates therefrom an output signal that is applied to a positive input terminal of adder 216 and to a negative input terminal of adder 218. Adder 216 generates a sum signal (indicated in Figure 3 as 'L+R') by summing the output signals generated by filters 212 and 214. Adder 218 generates a difference signal (indicated in Figure 3 as 'L-R') by subtracting the output signal generated by filter 214 from the output signal generated by filter 212. Input section 210 is therefore similar to input section 110 (shown in Figure 1) however, section 210 additionally includes the two high pass filters 212, 214 and generates digital sum and difference signals."

a sum and difference signal generator arrangement configured so as to generate a first pre-emphasized digital signal as a function of the summation signal, and a second pre-emphasized digital signal as a function of the difference signal;

Sum channel processing section 220 with 75 μs preemphasis filter is shown in Figure 3 and described in the specification at page 16, lines 22-25, "[r]eferring again to Figure 3, the sum channel processing section 220 receives the sum signal and generates therefrom the conditioned sum signal. In particular, the sum signal is applied to a 75 μs preemphasis filter 222." Difference channel processing section 230 with fixed preemphasis filter 232a and fixed preemphasis filter 232b is shown in Figure 3 and described in the specification at page 18, line 16-26, as follows, "[r]eferring again to Figure 3, the difference channel processing section 230 receives the difference signal and generates therefrom the encoded difference signal. The difference signal is applied to a low pass filter 238a which generates therefrom an output signal that is applied to a fixed preemphasis filter 232a. The latter generates an output signal that is applied via line 239 to an input terminal of a wideband compression unit 280, and the encoded difference signal is applied via feedback line 240 to a detector terminal of wideband compression unit 280. The latter generates an output signal that is applied via line 281 to an input terminal of a spectral compression unit 290, and the encoded difference signal is also applied via feedback line 240 to a detector terminal of unit 290. The latter generates an output

signal that is applied to a fixed preemphasis filter 232b which in turn generates an output signal that is applied to a clipper 254."

a signal transformation arrangement configured so as to transform the first pre-emphasized digital signal to a digital BTSC compliant L+R signal, and transform the second pre-emphasized digital signal to a digital BTSC compliant L-R signal;

Sum channel processing section 220 is described at page 16, lines 22-23, as follows, "[r]eferring again to Figure 3, the sum channel processing section 220 receives the sum signal and generates therefrom the conditioned sum signal." Difference channel processing section 230 is shown in Figure 3 and described at page 18, lines 16-17, as follows, "[r]eferring again to Figure 3, the difference channel processing section 230 receives the difference signal and generates therefrom the encoded difference signal." Sum channel processing section 220 and difference channel processing section 230 are also shown in Figure 8A. "[r]eferring again to Figure 3, the difference channel processing section 230 receives the difference signal and generates therefrom the encoded difference signal. The difference signal is applied to a low pass filter 238a which generates therefrom an output signal that is applied to a fixed preemphasis filter 232a. The latter generates an output signal that is applied via line 239 to an input terminal of a wideband compression unit 280, and the encoded difference signal is applied via feedback line 240 to a detector terminal of wideband compression unit 280. The latter generates an output signal that is applied via line 281 to an input terminal of a spectral compression unit 290, and the encoded difference signal is also applied via feedback line 240 to a detector terminal of unit 290. The latter generates an output signal that is applied to a fixed preemphasis filter 232b which in turn generates an output signal that is applied to a clipper 254."

transforming the first pre-emphasized digital signal to a digital BTSC compliant L+R signal and transforming the second pre-emphasized digital signal to a digital BTSC compliant L-R signal, wherein the difference between the digital BTSC compliant L+R signal and the digital BTSC compliant L-R signal, for a given frequency and level, conforms with the difference specified by the BTSC standard; and

Sum channel processing section 220 is shown in Figure 3 and described at page 16, lines 22-23, "[r]eferring again to Figure 3, the sum channel processing section 220 receives the sum

signal and generates therefrom the conditioned sum signal." Difference channel processing section 230 is shown in Figure 3 and described at page 18, lines 16-17, "[r]eferring again to Figure 3, the difference channel processing section 230 receives the difference signal and generates therefrom the encoded difference signal." Sum channel processing section 220 and difference channel processing section 230 are also shown in Figure 8A. The paragraph at page 14, lines 17-20, states in part that "[f]igure 3 is a block diagram of one embodiment of a digital BTSC encoder 200 constructed according to the invention. Digital encoder 200 is constructed to provide performance that is functionally equivalent to the performance of idealized encoder 100 (shown in Figure 1)" [Emphasis added].

a digital-to-analog converter arrangement configured to convert the digital BTSC compliant L+R signal to an analog BTSC compliant L+R signal, and the digital BTSC compliant L-R signal to an analog BTSC compliant L-R signal; and

Digital-to-analog converters 814 and 816 are shown Figure 8A and described in the specification on page 36, lines 16-18, and on page 37, lines 5-7, as follows: "The output signal generated by module 296 is applied to a sixteen bit digital-to-analog converter 814 which in turn generates an analog conditioned sum signal." "Referring again to Figure 8A, the output signal generated by filter 238b is applied to a sixteen bit digital-to-analog converter 816 which in turn generates an output signal that is applied to a 6 dB analog amplifier 820."

a composite signal generator arrangement configured so as to generate a composite signal as a function of the combination of the analog BTSC compliant L+R signal and a modulated version of the analog BTSC compliant L-R signal.

Signal adder 940 is shown in Figure 8D and described on page 42, lines 2-4, as follows, "The signals generated by attenuator 936 and amplifier 938 are applied to input terminals of signal adder 940 which sums these signals to generate the analog composite signal."

Claim 137

Independent claim 137 recites method of generating a broadcast television stereo signal from a left-channel signal and a right-channel signal, comprising:

As shown in Figure 8A and described in the specification at page 35, lines 6-7, "[f]igure 8A shows a block diagram that illustrates one method of using the DSP Embodiment in an analog system . . ." and at page 35, lines 8-10, "[t]he analog system supplies analog left and right channel audio input signals (shown in Figure 8A as 'L' and 'R', respectively) . . . ."

converting the right-channel signal to a right digital signal and converting the left-channel signal to a left digital signal;

As shown in Figure 8A and described in the specification at page 35, lines 11-14, "[c]onverters 810, 812 sample their analog input signals using a frequency f_S that is equal to 47,202 Hz (i.e., $3f_H$) and converters 810, 812 thereby generate sequences of sixteen bit digital samples that are representative of the left and right channel audio input signals, respectively."

generating a summation signal comprising the sum of the right digital signal and the left digital signal, and generating a difference signal comprising the difference between the right digital signal and the left digital signal;

As shown in Figure 3, and described on page 15, line 23 through page 16, line 7, "[t]he input section 210 of encoder 200 includes two high pass filters 212, 214, and two signal adders 216, 218. The left channel digital audio input signal L is applied to the input of high pass filter 212, the latter generating therefrom an output signal that is applied to positive input terminals of adders 216, 218. The right channel audio input signal R is applied to the input of high pass filter 214 which generates therefrom an output signal that is applied to a positive input terminal of adder 216 and to a negative input terminal of adder 218. Adder 216 generates a sum signal (indicated in Figure 3 as 'L+R') by summing the output signals generated by filters 212 and 214. Adder 218 generates a difference signal (indicated in Figure 3 as 'L-R') by subtracting the output signal generated by filter 214 from the output signal generated by filter 212. Input section 210 is therefore similar to input section 110 (shown in Figure 1) however, section 210 additionally includes the two high pass filters 212, 214 and generates digital sum and difference signals."

generating a first pre-emphasized digital signal as a function of the summation signal, and generating a second pre-emphasized digital signal as a function of the difference signal;

As shown in Figure 3 for 75 μs preemphasis filter 222, fixed preemphasis filter 232a, and fixed preemphasis filter 232b and described on page 16, lines 22-27, "[r]eferring again to Figure 3, the sum channel processing section 220 receives the sum signal and generates therefrom the conditioned sum signal. In particular, the sum signal is applied to a 75 μs preemphasis filter 222. The filter 222 in turn generates an output signal that is applied to a static phase equalization filter 228. The filter 228 generates an output signal that is applied to a low pass filter 224 of section 220 which in turn generates the conditioned sum signal." And, again, at page 18, lines 16-26, "[r]eferring again to Figure 3, the difference channel processing section 230 receives the difference signal and generates therefrom the encoded difference signal. The difference signal is applied to a low pass filter 238a which generates therefrom an output signal that is applied to a fixed preemphasis filter 232a. The latter generates an output signal that is applied via line 239 to an input terminal of a wideband compression unit 280, and the encoded difference signal is applied via feedback line 240 to a detector terminal of wideband compression unit 280. The latter generates an output signal that is applied via line 281 to an input terminal of a spectral compression unit 290, and the encoded difference signal is also applied via feedback line 240 to a detector terminal of unit 290. The latter generates an output signal that is applied to a fixed preemphasis filter 232b which in turn generates an output signal that is applied to a clipper 254."

transforming the first pre-emphasized digital signal to a digital BTSC compliant L+R signal and transforming the second pre-emphasized digital signal to a digital BTSC compliant L-R signal;

Sum channel processing section 220 is shown in Figure 3 and described at page 16, lines 22-23, "[r]eferring again to Figure 3, the sum channel processing section 220 receives the sum signal and generates therefrom the conditioned sum signal." Difference channel processing section 230 is shown in Figure 3 and described at page 18, lines 16-17, "[r]eferring again to Figure 3, the difference channel processing section 230 receives the difference signal and generates therefrom the encoded difference signal." Sum channel processing section 220 and difference channel processing section 230 are also shown in Figure 8A. The paragraph at page 14, lines 17-20, states in part that "[f]igure 3 is a block diagram of one embodiment of a digital BTSC encoder 200 constructed according to the invention. Digital encoder 200 is constructed to

provide performance that is functionally equivalent to the performance of idealized encoder 100 (shown in Figure 1)" [Emphasis added].

converting the digital BTSC compliant L+R signal to an analog BTSC compliant L+R signal, and converting the digital BTSC compliant L-R signal to an analog BTSC compliant L-R signal; and

As shown in Figure 8A, and described for digital-to-analog converter 814 on page 36, lines 16-18, "[t]he output signal generated by module 296 is applied to a sixteen bit digital-to-analog converter 814 which in turn generates an analog conditioned sum signal." And as shown in Figure 8A, and described on page 37, lines 5-7, for digital-to-analog converter 816, "[r]eferring again to Figure 8A, the output signal generated by filter 238b is applied to a sixteen bit digital-to-analog converter 816 which in turn generates an output signal that is applied to a 6 dB analog amplifier 820."

generating a composite signal as a function of a combination of the analog BTSC compliant L+R signal and a modulated version of the analog BTSC compliant L-R signal.

As shown in Figure 8D and described for signal adder 940 on page 42, lines 2-4, "[t]he signals generated by attenuator 936 and amplifier 938 are applied to input terminals of signal adder 940 which sums these signals to generate the analog composite signal."

Claim 141

Independent claim 141 recites method of generating a broadcast television stereo signal from a left-channel signal and a right-channel signal, the method comprising:

As shown in Figure 8A and described in the specification at page 35, lines 6-7, "[f]igure 8A shows a block diagram that illustrates one method of using the DSP Embodiment in an analog system . . ." and at page 35, lines 8-10, "[t]he analog system supplies analog left and right channel audio input signals (shown in Figure 8A as 'L' and 'R', respectively) . . . ."

converting the right-channel signal to a right digital signal;

As shown in Figure 8A and described in the specification at page 35, lines 11-14, "[c]onverters 810, 812 sample their analog input signals using a frequency f_S that is equal to 47,202 Hz (i.e., $3f_H$) and converters 810, 812 thereby generate sequences of sixteen bit digital samples that are representative of the left and right channel audio input signals, respectively."

converting the left-channel signal to a left digital signal;

As shown in Figure 8A and described in the specification at page 35, lines 11-14, "[c]onverters 810, 812 sample their analog input signals using a frequency f_S that is equal to 47,202 Hz (i.e., $3f_H$) and converters 810, 812 thereby generate sequences of sixteen bit digital samples that are representative of the left and right channel audio input signals, respectively."

generating a summation signal comprising the sum of the right digital signal and the left digital signal;

As shown in Figure 3, and described on page 16, lines 1-2, "[a]dder 216 generates a sum signal (indicated in Figure 3 as 'L+R') by summing the output signals generated by filters 212 and 214."

generating a difference signal comprising the difference between the right digital signal and the left digital signal;

As shown in Figure 3, and described on page 16, lines 2-4 "[a]dder 218 generates a difference signal (indicated in Figure 3 as 'L-R') by subtracting the output signal generated by filter 214 from the output signal generated by filter 212."

generating a first pre-emphasized digital signal corresponding to the summation signal;

As shown in Figure 3 for 75 μs preemphasis filter 222, fixed preemphasis filter 232a, and fixed preemphasis filter 232b and described on page 16, lines 22-27, "[r]eferring again to Figure 3, the sum channel processing section 220 receives the sum signal and generates therefrom the conditioned sum signal. In particular, the sum signal is applied to a 75 μs preemphasis filter 222. The filter 222 in turn generates an output signal that is applied to a static phase equalization filter 228. The filter 228 generates an output signal that is applied to a low pass filter 224 of section 220 which in turn generates the conditioned sum signal."

generating a second pre-emphasized digital signal corresponding to the difference signal;

As shown in Figure 3, and at page 18, lines 16-26, "[r]eferring again to Figure 3, the difference channel processing section 230 receives the difference signal and generates therefrom the encoded difference signal. The difference signal is applied to a low pass filter 238a which generates therefrom an output signal that is applied to a fixed preemphasis filter 232a. The latter generates an output signal that is applied via line 239 to an input terminal of a wideband compression unit 280, and the encoded difference signal is applied via feedback line 240 to a detector terminal of wideband compression unit 280. The latter generates an output signal that is applied via line 281 to an input terminal of a spectral compression unit 290, and the encoded difference signal is also applied via feedback line 240 to a detector terminal of unit 290. The latter generates an output signal that is applied to a fixed preemphasis filter 232b which in turn generates an output signal that is applied to a clipper 254."

transforming the first pre-emphasized digital signal to a digital BTSC compliant L+R signal;

Sum channel processing section 220 is described at page 16, lines 22-23, as follows, "[r]eferring again to Figure 3, the sum channel processing section 220 receives the sum signal and generates therefrom the conditioned sum signal."

transforming the second pre-emphasized digital signal to a digital BTSC compliant L-R signal;

Difference channel processing section 230 is shown in Figure 3 and described at page 18, lines 16-17, as follows, "[r]eferring again to Figure 3, the difference channel processing section 230 receives the difference signal and generates therefrom the encoded difference signal." Sum channel processing section 220 and difference channel processing section 230 are also shown in Figure 8A.

converting the digital BTSC compliant L+R signal to an analog BTSC compliant L+R signal;

As shown in Figure 8A, and described on page 36, lines 10-18, for digital-to-analog converter 814, "[i]nput section 210 receives the twenty-four bit words generated by modules 292, 294 and generates therefrom the sum signal that is applied to the sum channel processing section 220. The output signal generated by sum channel processing section 220 is applied to a 'times 16 module' (which may be considered as a 24 dB amplifier) 296. Module 296 thereby compensates for the -24dB attenuators 292, 294 and brings the output of sum channel processing section 220 back to 100% modulation (i.e., back to 'full scale'). The output signal generated by module 296 is applied to a sixteen bit digital-to analog converter 814 which in turn generates an analog conditioned sum signal."

converting the digital BTSC compliant L-R signal to an analog BTSC compliant L-R signal; and

As shown in Figure 8A, and described on page 36, lines 19-20, "[i]nput section 210 also generates the difference signal that is applied to the difference channel processing section 230" and in the same paragraph on page 37, lines 5-7, for digital-to-analog converter 816, "[r]eferring again to Figure 8A, the output signal generated by filter 238b is applied to a sixteen bit digital-to-analog converter 816 which in turn generates an output signal that is applied to a 6 dB analog amplifier 820."

generating a composite signal as a function of a combination of the analog BTSC compliant L+R signal with a modulated version of the analog BTSC compliant L-R signal.

As shown in Figure 8D and described for signal adder 940 on page 42, lines 2-4, "[t]he signals generated by attenuator 936 and amplifier 938 are applied to input terminals of signal adder 940 which sums these signals to generate the analog composite signal."

Claim 143

Independent claim 143 recites system for generating a broadcast television stereo signal from a left-channel signal and a right-channel signal, comprising:

Figure 8A and as described on page 35, lines 6-11, "[f]igure 8A shows a block diagram that illustrates one method of using the DSP Embodiment in an analog system. . . . The analog

system supplies analog left and right channel audio input signals (shown in Figure 8A as 'L' and 'R', respectively) . . . ."

an analog-to-digital converter arrangement configured so as to convert the right-channel signal to a right digital signal and convert the left-channel signal to a left digital signal;

As shown in Figure 8A, and as described in the paragraph at page 35, lines 8-14, "[t]he analog system supplies analog left and right channel audio input signals (shown in Figure 8A as 'L' and 'R,' respectively) and these signals are applied to the inputs of sixteen bit analog-to-digital converters 810 and 812, respectively. Converters 810, 812 sample their analog input signals using a sampling frequency f_S that is equal to 47,202 Hz (i.e., $3f_H$) and converters 810, 812 thereby generate sequences of sixteen bit digital samples that are representative of the left and right channel audio input signals, respectively."

a signal combiner arrangement coupled to the analog-to-digital converter arrangement and configured so as to generate a summation signal comprising the sum of the right digital signal and the left digital signal, and generate a difference signal comprising the difference between the right digital signal and the left digital signal;

As described in the paragraph at page 35, lines 14-16, "[t]he signals generated by converters 810 and 812 are applied to encoder 200a where they are received by modules 292 and 294, respectively." The paragraph at page 36, lines 10-12, states, "[i]nput section 210 receives the twenty-four bit words generated by modules 292, 294 and generates therefrom the sum signal that is applied to the sum channel processing section 220 ." The paragraph at page 36, lines 19-21, further states, "[i]nput section 210 also generates the difference signal that is applied to the difference channel processing section 230. As states above, as a result of modules 292, 294, the difference signal may be considered as being attenuated by 24 dB."

a sum and difference signal generator arrangement configured so as to generate a first pre-emphasized digital signal as a function of the summation signal, and a second pre-emphasized digital signal as a function of the difference signal;

Sum channel processing section 220 with 75 μs preemphasis filter is shown in Figure 3 and described in the specification at page 16, lines 22-25, "[r]eferring again to Figure 3, the

sum channel processing section 220 receives the sum signal and generates therefrom the conditioned sum signal. In particular, the sum signal is applied to a 75 μs preemphasis filter 222." Difference channel processing section 230 with fixed preemphasis filter 232a and fixed preemphasis filter 232b is shown in Figure 3 and described in the specification at page 18, line 16-26, as follows, "[r]eferring again to Figure 3, the difference channel processing section 230 receives the difference signal and generates therefrom the encoded difference signal. The difference signal is applied to a low pass filter 238a which generates therefrom an output signal that is applied to a fixed preemphasis filter 232a. The latter generates an output signal that is applied via line 239 to an input terminal of a wideband compression unit 280, and the encoded difference signal is applied via feedback line 240 to a detector terminal of wideband compression unit 280. The latter generates an output signal that is applied via line 281 to an input terminal of a spectral compression unit 290, and the encoded difference signal is also applied via feedback line 240 to a detector terminal of unit 290. The latter generates an output signal that is applied to a fixed preemphasis filter 232b which in turn generates an output signal that is applied to a clipper 254."

a signal transformation arrangement configured so as to transform the first pre-emphasized digital signal to a digital BTSC compliant L+R signal, and transform the second pre-emphasized digital signal to a digital BTSC compliant L-R signal;

Sum channel processing section 220 is described at page 16, lines 22-23, as follows, "[r]eferring again to Figure 3, the sum channel processing section 220 receives the sum signal and generates therefrom the conditioned sum signal." Difference channel processing section 230 is shown in Figure 3 and described at page 18, lines 16-17, as follows, "[r]eferring again to Figure 3, the difference channel processing section 230 receives the difference signal and generates therefrom the encoded difference signal." Sum channel processing section 220 and difference channel processing section 230 are also shown in Figure 8A.

a composite signal generator arrangement configured so as to generate a digital composite signal as a function of the combination of the digital BTSC compliant L+R signal and a modulated version of the digital BTSC compliant L-R signal; and

As shown in Figure 8B and described on page 37, lines 21-23, "[f]igure 8B shows a block diagram of one preferred embodiment of a BTSC encoder 200b constructed according to the invention and configured as part of an analog system. Encoder 200b is similar to encoder 200a . . ." and on page 38, lines 2-4, "encoder 200b includes a composite modulator 822 for receiving the signals S and D and for generating therefrom a digital version of the composite signal."

a digital-to-analog converter arrangement configured to convert the digital composite signal to an analog composite signal.

Digital-to-analog converters 814 and 816 are shown Figure 8A and described in the specification on page 36, lines 16-18, and on page 37, lines 5-7, as follows: "The output signal generated by module 296 is applied to a sixteen bit digital-to-analog converter 814 which in turn generates an analog conditioned sum signal." "Referring again to Figure 8A, the output signal generated by filter 238b is applied to a sixteen bit digital-to-analog converter 816 which in turn generates an output signal that is applied to a 6 dB analog amplifier 820."

Claim 146

Independent claim 146 recites a method of generating a broadcast television stereo signal from a left-channel signal and a right-channel signal, comprising:

As shown in Figure 8A and described in the specification at page 35, lines 6-7, "[f]igure 8A shows a block diagram that illustrates one method of using the DSP Embodiment in an analog system . . ." and at page 35, lines 8-10, "[t]he analog system supplies analog left and right channel audio input signals (shown in Figure 8A as 'L' and 'R', respectively) . . . ."

converting the right-channel signal to a right digital signal and converting the left-channel signal to a left digital signal;

As shown in Figure 8A and described in the specification at page 35, lines 11-14, "[c]onverters 810, 812 sample their analog input signals using a frequency f_S that is equal to 47,202 Hz (i.e., $3f_H$) and converters 810, 812 thereby generate sequences of sixteen bit digital samples that are representative of the left and right channel audio input signals, respectively."

generating a summation signal comprising the sum of the right digital signal and the left digital signal, and generating a difference signal comprising the difference between the right digital signal and the left digital signal;

As shown in Figure 3, and described on page 15, line 23 through page 16, line 7, "[t]he input section 210 of encoder 200 includes two high pass filters 212, 214, and two signal adders 216, 218. The left channel digital audio input signal L is applied to the input of high pass filter 212, the latter generating therefrom an output signal that is applied to positive input terminals of adders 216, 218. The right channel audio input signal R is applied to the input of high pass filter 214 which generates therefrom an output signal that is applied to a positive input terminal of adder 216 and to a negative input terminal of adder 218. Adder 216 generates a sum signal (indicated in Figure 3 as 'L+R') by summing the output signals generated by filters 212 and 214. Adder 218 generates a difference signal (indicated in Figure 3 as 'L-R') by subtracting the output signal generated by filter 214 from the output signal generated by filter 212. Input section 210 is therefore similar to input section 110 (shown in Figure 1) however, section 210 additionally includes the two high pass filters 212, 214 and generates digital sum and difference signals."

generating a first pre-emphasized digital signal as a function of the summation signal, and generating a second pre-emphasized digital signal as a function of the difference signal;

As shown in Figure 3 for 75 μs preemphasis filter 222, fixed preemphasis filter 232a, and fixed preemphasis filter 232b and described on page 16, lines 22-27, "[r]eferring again to Figure 3, the sum channel processing section 220 receives the sum signal and generates therefrom the conditioned sum signal. In particular, the sum signal is applied to a 75 μs preemphasis filter 222. The filter 222 in turn generates an output signal that is applied to a static phase equalization filter 228. The filter 228 generates an output signal that is applied to a low pass filter 224 of section 220 which in turn generates the conditioned sum signal"; as shown in Figure 3, and at page 18, lines 16-26, "[r]eferring again to Figure 3, the difference channel processing section 230 receives the difference signal and generates therefrom the encoded difference signal. The difference signal is applied to a low pass filter 238a which generates

therefrom an output signal that is applied to a fixed preemphasis filter 232a. The latter generates an output signal that is applied via line 239 to an input terminal of a wideband compression unit 280, and the encoded difference signal is applied via feedback line 240 to a detector terminal of wideband compression unit 280. The latter generates an output signal that is applied via line 281 to an input terminal of a spectral compression unit 290, and the encoded difference signal is also applied via feedback line 240 to a detector terminal of unit 290. The latter generates an output signal that is applied to a fixed preemphasis filter 232b which in turn generates an output signal that is applied to a clipper 254."

transforming the first pre-emphasized digital signal to a digital BTSC compliant L+R signal and transforming the second pre-emphasized digital signal to a digital BTSC compliant L-R signal;

Sum channel processing section 220 is described at page 16, lines 22-23, as follows, "[r]eferring again to Figure 3, the sum channel processing section 220 receives the sum signal and generates therefrom the conditioned sum signal." Difference channel processing section 230 is shown in Figure 3 and described at page 18, lines 16-17, as follows, "[r]eferring again to Figure 3, the difference channel processing section 230 receives the difference signal and generates therefrom the encoded difference signal." Sum channel processing section 220 and difference channel processing section 230 are also shown in Figure 8A.

generating a digital composite signal as a function of a combination of the digital BTSC compliant L+R signal and a modulated version of the digital BTSC compliant L-R signal; and

As shown in Figure 8B, and described on page 37, lines 21-23, "[f]igure 8B shows a block diagram of one preferred embodiment of a BTSC encoder 200b constructed according to the invention and configured as part of an analog system. Encoder 200b is similar to encoder 200a . . . ." As also described on page 37, line 25 to page 38, line 6, "[t]he output signal generated by module 296 is a scaled version of the conditioned sum signal and is shown in Figure 8B as S. Also, encoder 200b includes a module 298 for amplifying the output signal generated by difference channel processing section 230 by 6 dB (by multiplying by two). The output signal generated by module 298 is a scaled version of the encoded difference signal and is

shown in Figure 8B as D. Further, encoder 200b includes a composite modulator 822 for receiving the signals S and D and for generating therefrom a digital version of the composite signal.

converting the digital composite signal to an analog composite signal.

As shown in Figure 8C, and described on page 40, lines 9-11, "[t]his attenuated version of the composite signal is converted to an analog signal by digital-to-analog converter 818 . . . ."

Claim 150

Independent claim 150 recites a method of generating a broadcast television stereo signal from a left-channel signal and a right-channel signal, the method comprising:

As shown in Figure 8A and described in the specification at page 35, lines 6-7, "[f]igure 8A shows a block diagram that illustrates one method of using the DSP Embodiment in an analog system . . ." and at page 35, lines 8-10, "[t]he analog system supplies analog left and right channel audio input signals (shown in Figure 8A as 'L' and 'R', respectively) . . . ."

converting the right-channel signal to a right digital signal;

As shown in Figure 8A and described in the specification at page 35, lines 11-14, "[c]onverters 810, 812 sample their analog input signals using a frequency f_S that is equal to 47,202 Hz (i.e., $3f_H$) and converters 810, 812 thereby generate sequences of sixteen bit digital samples that are representative of the left and right channel audio input signals, respectively."

converting the left-channel signal to a left digital signal;

As shown in Figure 8A and described in the specification at page 35, lines 11-14, "[c]onverters 810, 812 sample their analog input signals using a frequency f_S that is equal to 47,202 Hz (i.e., $3f_H$) and converters 810, 812 thereby generate sequences of sixteen bit digital samples that are representative of the left and right channel audio input signals, respectively."

generating a summation signal comprising the sum of the right digital signal and the left digital signal;

As shown in Figure 3, and described on page 16, lines 1-2, "[a]dder 216 generates a sum signal (indicated in Figure 3 as 'L+R') by summing the output signals generated by filters 212 and 214."

generating a difference signal comprising the difference between the right digital signal and the left digital signal;

As shown in Figure 3, and described on page 16, lines 2-4 "[a]dder 218 generates a difference signal (indicated in Figure 3 as 'L-R') by subtracting the output signal generated by filter 214 from the output signal generated by filter 212."

generating a first pre-emphasized digital signal corresponding to the summation signal;

As shown in Figure 3 for 75 μs preemphasis filter 222, fixed preemphasis filter 232a, and fixed preemphasis filter 232b and described on page 16, lines 22-27, "[r]eferring again to Figure 3, the sum channel processing section 220 receives the sum signal and generates therefrom the conditioned sum signal. In particular, the sum signal is applied to a 75 μs preemphasis filter 222. The filter 222 in turn generates an output signal that is applied to a static phase equalization filter 228. The filter 228 generates an output signal that is applied to a low pass filter 224 of section 220 which in turn generates the conditioned sum signal."

generating a second pre-emphasized digital signal corresponding to the difference signal;

As shown in Figure 3, and at page 18, lines 16-26, "[r]eferring again to Figure 3, the difference channel processing section 230 receives the difference signal and generates therefrom the encoded difference signal. The difference signal is applied to a low pass filter 238a which generates therefrom an output signal that is applied to a fixed preemphasis filter 232a. The latter generates an output signal that is applied via line 239 to an input terminal of a wideband compression unit 280, and the encoded difference signal is applied via feedback line 240 to a detector terminal of wideband compression unit 280. The latter generates an output signal that is applied via line 281 to an input terminal of a spectral compression unit 290, and the encoded difference signal is also applied via feedback line 240 to a detector terminal of unit 290. The

latter generates an output signal that is applied to a fixed preemphasis filter 232b which in turn generates an output signal that is applied to a clipper 254."

transforming the first pre-emphasized digital signal to a digital BTSC compliant L+R signal;

Sum channel processing section 220 is described at page 16, lines 22-23, as follows, "[r]eferring again to Figure 3, the sum channel processing section 220 receives the sum signal and generates therefrom the conditioned sum signal."

transforming the second pre-emphasized digital signal to a digital BTSC compliant L-R signal;

Difference channel processing section 230 is shown in Figure 3 and described at page 18, lines 16-17, as follows, "[r]eferring again to Figure 3, the difference channel processing section 230 receives the difference signal and generates therefrom the encoded difference signal." Sum channel processing section 220 and difference channel processing section 230 are also shown in Figure 8A.

generating a digital composite signal as a function of a combination of the digital BTSC compliant L+R signal with a modulated version of the digital BTSC compliant L-R signal; and

As shown in Figure 8B, and described on page 37, lines 21-23, "[f]igure 8B shows a block diagram of one preferred embodiment of a BTSC encoder 200b constructed according to the invention and configured as part of an analog system. Encoder 200b is similar to encoder 200a . . . ." As also described on page 37, line 25 to page 38, line 6, "[t]he output signal generated by module 296 is a scaled version of the conditioned sum signal and is shown in Figure 8B as S. Also, encoder 200b includes a module 298 for amplifying the output signal generated by difference channel processing section 230 by 6 dB (by multiplying by two). The output signal generated by module 298 is a scaled version of the encoded difference signal and is shown in Figure 8B as D. Further, encoder 200b includes a composite modulator 822 for receiving the signals S and D and for generating therefrom a digital version of the composite signal.

converting the digital composite signal to an analog composite signal.

As shown in Figure 8C, and described on page 40, lines 9-11, "[t]his attenuated version of the composite signal is converted to an analog signal by digital-to-analog converter 818 . . . ."

Claim 152

Independent claim 152 recites a digital signal processor arrangement for use in generating a broadcast television BTSC encoded stereo signal from a left-channel signal and a right-channel signal, comprising:

As shown in Figure 3, and discussed on page 14, lines 17-23, "[f]igure 3 is a block diagram of one embodiment of a digital BTSC encoder 200 constructed according to the invention. Digital encoder 200 is constructed to provide performance that is functionally equivalent to the performance of idealized encoder 100 (shown in Figure 1). As with idealized encoder 100, digital encoder 200 receives the left and right channel audio input signals and generates therefrom the conditioned sum signal and the encoded difference signal, however, in digital encoder 200 these input and output signals are digitally sampled signals rather than continuous analog signals."

a signal generator arrangement configured so as to generate a digital summation signal as a function of the sum of the left-channel and right-channel signals, and a digital difference signal as a function of the difference between the left-channel and right-channel signals;

As described on 37, line 23, "encoder 200b is similar to encoder 200a" of Figure 8A; the paragraph at page 36, lines 10-11, explains that input section 210 of Figure 8A receives the L and R channels "and generates therefrom the sum signal that is applied to the sum channel processing section"; while the paragraph at page 36, lines 19-20, explains that "[i]nput section 210 also generates the difference signal that is applied to the difference channel processing section 230"; in a similar way, input section 210 of Figure 8B functions as a signal generator arrangement or matrix as it receives L and R signals and generates sum (L+R) and difference

(L-R) signals; the Abstract makes this clear by disclosing "a matrix means for receiving the digital left and digital right filtered signals, and including means for summing the digital left and digital right filtered signals and thereby generating a digital sum signal, and including means for subtracting one of the digital left and digital right filtered signals from the other of the digital left and digital right filtered signals and thereby generating a digital difference signal" [Emphasis added].

a summation signal processing arrangement including a filter arrangement configured to filter the digital summation signal so as to produce a conditioned digital summation signal;

The paragraph at page 37, line 23, states that encoder 200b is similar to encoder 200a of Figure 8A; Figure 8A shows that a conditioned sum signal is produced by the sum channel processing section block 220, which is a digital component and equivalent to a digital sum channel section; Figure 8B depicts "a sum channel processing section 220" block; Figure 3 and the paragraph at page 16, lines 22-27, disclose that the sum channel processing section 220 includes a 75 μs preemphasis filter, a static phase equalization filter 228, and a low pass filter 224; further, the paragraph at page 12, lines 17-19, discloses in part "an improved BTSC encoder that includes an input section, a sum channel processing section, and a difference channel processing section all of which are implemented using digital technology."

a difference signal processing arrangement including a pre-emphasis filter arrangement and a signal compressor arrangement, the filter and signal compressor arrangements being configured so as to condition and compress the digital difference signal so as to produce a conditioned digital difference signal;

The paragraph at page 37, line 23, states that encoder 200b is similar to encoder 200a of Figure 8A; Figure 8A shows that an encoded digital difference signal is produced by the difference channel processing section block 230; Figure 8B depicts "a difference channel processing section 230" block; Figure 3 and the paragraph at page 18, lines 16-26, state "the difference channel processing section 230 receives the difference signal and generates therefrom the encoded difference signal. The difference signal is applied to a low pass filter 238a which generates therefrom an output signal that is applied to a fixed preemphasis filter 232a. The latter

generates an output signal that is applied via line 239 to an input terminal of a wideband compression unit 280, and the encoded difference signal is applied via feedback line 240 to a detector terminal of wideband compression unit 280. The latter generates an output signal that is applied via line 281 to an input terminal of a spectral compression unit 290, and the encoded difference signal is also applied via feedback line 240 to a detector terminal of unit 290. The latter generates an output signal that is applied to a fixed preemphasis filter 232b which in turn generates an output signal that is applied to a clipper 254. Clipper 254 generates an output signal that is applied to a low pass filter 238b which in turn generates the encoded difference signal."

a digital-to-analog converter arrangement for converting the conditioned digital summation signal to an analog sum signal, and the conditioned digital difference signal to an analog difference signal; and

Digital-to-analog converters 814 and 816 are shown Figure 8A and described in the specification on page 36, lines 16-18, and on page 37, lines 5-7, as follows: "The output signal generated by module 296 is applied to a sixteen bit digital-to-analog converter 814 which in turn generates an analog conditioned sum signal." "Referring again to Figure 8A, the output signal generated by filter 238b is applied to a sixteen bit digital-to-analog converter 816 which in turn generates an output signal that is applied to a 6 dB analog amplifier 820."

a signal combiner arrangement configured so as to combine the analog sum signal with a modulated version of the analog difference signal.

Signal adder 940 is shown in Figure 8D and described on page 42, lines 2-4, as follows, "The signals generated by attenuator 936 and amplifier 938 are applied to input terminals of signal adder 940 which sums these signals to generate the analog composite signal."

Claim 154

Independent claim 154 recites a digital signal processor arrangement for use in generating a broadcast television BTSC encoded stereo signal from a left-channel signal and a right-channel signal, comprising:

As shown in Figure 3, and discussed on page 14, lines 17-23, "[f]igure 3 is a block diagram of one embodiment of a digital BTSC encoder 200 constructed according to the invention. Digital encoder 200 is constructed to provide performance that is functionally equivalent to the performance of idealized encoder 100 (shown in Figure 1). As with idealized encoder 100, digital encoder 200 receives the left and right channel audio input signals and generates therefrom the conditioned sum signal and the encoded difference signal, however, in digital encoder 200 these input and output signals are digitally sampled signals rather than continuous analog signals."

a signal generator arrangement configured so as to generate a digital summation signal as a function of the sum of the left-channel and right-channel signals, and a digital difference signal as a function of the difference between the left-channel and right-channel signals;

As described on 37, line 23, "encoder 200b is similar to encoder 200a" of Figure 8A; the paragraph at page 36, lines 10-11, explains that input section 210 of Figure 8A receives the L and R channels "and generates therefrom the sum signal that is applied to the sum channel processing section"; while the paragraph at page 36, lines 19-20, explains that "[i]nput section 210 also generates the difference signal that is applied to the difference channel processing section 230"; in a similar way, input section 210 of Figure 8B functions as a signal generator arrangement or matrix as it receives L and R signals and generates sum (L+R) and difference (L-R) signals; the Abstract makes this clear by disclosing "a matrix means for receiving the digital left and digital right filtered signals, and including means for summing the digital left and digital right filtered signals and thereby generating a digital sum signal, and including means for subtracting one of the digital left and digital right filtered signals from the other of the digital left and digital right filtered signals and thereby generating a digital difference signal" [Emphasis added].

a summation signal processing arrangement including a filter arrangement configured to filter the digital summation signal so as to produce a conditioned digital summation signal;

The paragraph at page 37, line 23, states that encoder 200b is similar to encoder 200a of Figure 8A; Figure 8A shows that a conditioned sum signal is produced by the sum channel processing section block 220, which is a digital component and equivalent to a digital sum channel section; Figure 8B depicts "a sum channel processing section 220" block; Figure 3 and the paragraph at page 16, lines 22-27, disclose that the sum channel processing section 220 includes a 75 μs preemphasis filter, a static phase equalization filter 228, and a low pass filter 224."

a difference signal processing arrangement including a pre-emphasis filter arrangement and a signal compressor arrangement, the filter and compressor arrangements being configured so as to condition and compress the digital difference signal so as to produce a conditioned digital difference signal;

The paragraph at page 37, line 23, states that encoder 200b is similar to encoder 200a of Figure 8A; Figure 8A shows that an encoded digital difference signal is produced by the difference channel processing section block 230; Figure 8B depicts "a difference channel processing section 230" block; Figure 3 and the paragraph at page 18, lines 16-26, state "the difference channel processing section 230 receives the difference signal and generates therefrom the encoded difference signal. The difference signal is applied to a low pass filter 238a which generates therefrom an output signal that is applied to a fixed preemphasis filter 232a. The latter generates an output signal that is applied via line 239 to an input terminal of a wideband compression unit 280, and the encoded difference signal is applied via feedback line 240 to a detector terminal of wideband compression unit 280. The latter generates an output signal that is applied via line 281 to an input terminal of a spectral compression unit 290, and the encoded difference signal is also applied via feedback line 240 to a detector terminal of unit 290. The latter generates an output signal that is applied to a fixed preemphasis filter 232b which in turn generates an output signal that is applied to a clipper 254. Clipper 254 generates an output signal that is applied to a low pass filter 238b which in turn generates the encoded difference signal."

a signal combiner arrangement configured so as to combine the conditioned digital summation signal with a modulated version of the conditioned digital difference signal so as to generate a composite modulated signal; and

Figures 8B and 9 show a composite modulator 822; the paragraph at page 38, lines 2-4, states in part that "encoder 200b includes a composite modulator 822 for receiving the signals S and D and for generating therefrom a digital version of the composite signal"; additionally, the paragraph at page 12, lines 10-12, discloses "a digital BTSC encoder including a composite modulator for generating a composite modulated signal from the conditioned sum signal and the encoded difference signal" [Emphasis added].

a digital-to-analog converter arrangement for converting the composite modulated signal to an analog output signal.

As shown in Figure 8B and described on page 37, lines 21 through page 38, line 6, "[f]igure 8B shows a block diagram of one preferred embodiment of a BTSC encoder 200b constructed according to the invention and configured as part of an analog system. Encoder 200b is similar to encoder 200a, however, in encoder 200b module 296 amplifies its input signal by 18 dB (by multiplying by 8) rather than by 24 dB as in encoder 200a. The output signal generated by module 296 is a scaled version of the conditioned sum signal and is shown in Figure 8B as S. Also, encoder 200b includes a module 298 for amplifying the output signal generated by difference channel processing section 230 by 6 dB (by multiplying by two). The output signal generated by module 298 is a scaled version of the encoded difference signal and is shown in Figure 8B as D. Further, encoder 200b includes a composite modulator 822 for receiving the signals S and D and for generating therefrom a digital version of the composite signal. The digital composite signal generated by modulator 822 is applied to a digital-to-analog converter 818 the output of which is an analog version of the composite signal."

Claim 156

Independent claim 156 recites a method of digitally encoding left and right channel audio signals in accordance with the BTSC standard, comprising:

The paragraph at page 35, lines 7-8, of the specification describes, in reference to Figure 8A, "[f]igure 8A shows a block diagram that illustrates one method of using the DSP embodiment . . . ."

providing digital left and digital right channel audio signals;

The paragraph at page 35, lines 9-11, of the specification describes, in reference to Figure 8A, "left and right channel audio input signals (shown in Figure 8A as 'L' and 'R,' respectively) and these signals are applied to the inputs of sixteen bit analog-to-digital converters 810 and 812, respectively"; this section of the specification along with Figure 8A provides support for the limitation of "generating digital left and digital right channel audio signals."

combining the digital left and digital right channel audio signals to form a digital sum signal and a digital difference signal; and

The paragraph at page 15, line 23 to page 16, line 7, of the specification describes, in reference to Figure 3, "[t]he input section 210 of encoder 200 includes two high pass filters 212, 214, and two signal adders 216, 218. The left channel digital audio input signal L is applied to the input of high pass filter 212, the latter generating therefrom an output signal that is applied to positive input terminals of adders 216, 218. The right channel audio input signal R is applied to the input of high pass filter 214 which generates therefrom an output signal that is applied to a positive input terminal of adder 216 and to a negative input terminal of adder 218. Adder 216 generates a sum signal (indicated in Figure 3 as 'L+R') by summing the output signals generated by filters 212 and 214. Adder 218 generates a difference signal (indicated in Figure 3 as 'L-R') by subtracting the output signal generated by filter 214 from the output signal generated by filter 212."

encoding the digital sum signal and the digital difference signal according to the BTSC standard so as to produce a digital BTSC signal.

As shown in Figure 3 for 75 μs preemphasis filter 222, fixed preemphasis filter 232a, and fixed preemphasis filter 232b and described on page 16, lines 22-27, "[r]eferring again to Figure 3, the sum channel processing section 220 receives the sum signal and generates

therefrom the conditioned sum signal. In particular, the sum signal is applied to a 75 μs preemphasis filter 222. The filter 222 in turn generates an output signal that is applied to a static phase equalization filter 228. The filter 228 generates an output signal that is applied to a low pass filter 224 of section 220 which in turn generates the conditioned sum signal." And, again, at page 18, lines 16-26, "[r]eferring again to Figure 3, the difference channel processing section 230 receives the difference signal and generates therefrom the encoded difference signal."

Claim 160

Independent claim 160 recites a digital signal processor for producing a signal encoded according to the BTSC standard, said digital signal processor comprising:

As shown in Figure 3, and discussed on page 14, lines 17-23, "[f]igure 3 is a block diagram of one embodiment of a digital BTSC encoder 200 constructed according to the invention. Digital encoder 200 is constructed to provide performance that is functionally equivalent to the performance of idealized encoder 100 (shown in Figure 1). As with idealized encoder 100, digital encoder 200 receives the left and right channel audio input signals and generates therefrom the conditioned sum signal and the encoded difference signal, however, in digital encoder 200 these input and output signals are digitally sampled signals rather than continuous analog signals."

A) an input section constructed and arranged so as to (1) receive digital left and digital right audio signals and (2) combine the digital left and digital right audio signals so as to form a digital sum signal and a digital difference signal;

As described on 37, line 23, "encoder 200b is similar to encoder 200a" of Figure 8A; the paragraph at page 36, lines 10-11, explains that input section 210 of Figure 8A receives the L and R channels "and generates therefrom the sum signal that is applied to the sum channel processing section"; while the paragraph at page 36, lines 19-20, explains that "[i]nput section 210 also generates the difference signal that is applied to the difference channel processing section 230"; in a similar way, input section 210 of Figure 8B functions as a signal generator

arrangement or matrix as it receives L and R signals and generates sum (L+R) and difference (L-R) signals."

B) a difference channel processing section constructed and arranged so as to encode the digital difference signal according to the BTSC standard; and

The paragraph at page 37, line 23, states that encoder 200b is similar to encoder 200a of Figure 8A; Figure 8A shows that an encoded digital difference signal is produced by the difference channel processing section block 230; Figure 8B depicts "a difference channel processing section 230" block; Figure 3 and the paragraph at page 18, lines 16-26, state "the difference channel processing section 230 receives the difference signal and generates therefrom the encoded difference signal. The difference signal is applied to a low pass filter 238a which generates therefrom an output signal that is applied to a fixed preemphasis filter 232a. The latter generates an output signal that is applied via line 239 to an input terminal of a wideband compression unit 280, and the encoded difference signal is applied via feedback line 240 to a detector terminal of wideband compression unit 280. The latter generates an output signal that is applied via line 281 to an input terminal of a spectral compression unit 290, and the encoded difference signal is also applied via feedback line 240 to a detector terminal of unit 290. The latter generates an output signal that is applied to a fixed preemphasis filter 232b which in turn generates an output signal that is applied to a clipper 254. Clipper 254 generates an output signal that is applied to a low pass filter 238b which in turn generates the encoded difference signal."

C) a sum channel processing section constructed and arranged so as to condition the digital sum signal according to the BTSC standard.

The paragraph at page 37, line 23, states that encoder 200b is similar to encoder 200a of Figure 8A; Figure 8A shows that a conditioned sum signal is produced by the sum channel processing section block 220, which is a digital component and equivalent to a digital sum channel section; Figure 8B depicts "a sum channel processing section 220" block; Figure 3 and the paragraph at page 16, lines 22-27, disclose that the sum channel processing section 220 includes a 75 μs preemphasis filter, a static phase equalization filter 228, and a low pass filter 224; further, the paragraph at page 12, lines 17-19, discloses in part "an improved BTSC

encoder that includes an input section, a sum channel processing section, and a difference channel processing section all of which are implemented using digital technology.

Claim 161

Independent claim 161 recites a system for producing a digital composite modulated BTSC signal comprising a digital BTSC encoder arranged so as to generate a digital BTSC encoded signal, and a digital composite modulator.

The paragraph at page 35, lines 7-8, of the specification describes, in reference to Figure 8A, "[f]igure 8A shows a block diagram that illustrates one method of using the DSP embodiment . . . . As shown in Figure 9, and described on page 38, lines 21-23, "[f]igure 9 shows a block diagram of one embodiment of composite modulator 822. The latter receives the signals S and D and generates therefrom a digital version of the composite signal."

Claim 162

Independent claim 162 recites a method of generating a digital composite modulated BTSC signal, comprising:

The paragraph at page 35, lines 7-8, of the specification describes, in reference to Figure 8A, "[f]igure 8A shows a block diagram that illustrates one method of using the DSP embodiment . . . ."

generating digital left and digital right channel audio signals,

The paragraph at page 35, lines 9-11, of the specification describes, in reference to Figure 8A, "left and right channel audio input signals (shown in Figure 8A as 'L' and 'R,' respectively) and these signals are applied to the inputs of sixteen bit analog-to-digital converters 810 and 812, respectively"; this section of the specification along with Figure 8A provides support for the limitation of "generating digital left and digital right channel audio signals."

combining said digital left and digital right channel audio signals so as to form a digital sum signal and a digital difference signal,

The paragraph at page 15, line 23 to page 16, line 7, of the specification describes, in reference to Figure 3, "[t]he input section 210 of encoder 200 includes two high pass filters 212, 214, and two signal adders 216, 218. The left channel digital audio input signal L is applied to the input of high pass filter 212, the latter generating therefrom an output signal that is applied to positive input terminals of adders 216, 218. The right channel audio input signal R is applied to the input of high pass filter 214 which generates therefrom an output signal that is applied to a positive input terminal of adder 216 and to a negative input terminal of adder 218. Adder 216 generates a sum signal (indicated in Figure 3 as 'L+R') by summing the output signals generated by filters 212 and 214. Adder 218 generates a difference signal (indicated in Figure 3 as 'L-R') by subtracting the output signal generated by filter 214 from the output signal generated by filter 212".

encoding the digital sum signal and digital difference signal according to the BTSC standard so as to produce a digital BTSC signal, and

The paragraph at page 37, line 23, states that encoder 200b is similar to encoder 200a of Figure 8A; Figure 8A shows that a conditioned sum signal is produced by the sum channel processing section block 220, which is a digital component and equivalent to a digital sum channel section; Figure 8B depicts "a sum channel processing section 220" block; Figure 3 and the paragraph at page 16, lines 22-27, disclose that the sum channel processing section 220 includes a 75 μs preemphasis filter, a static phase equalization filter 228, and a low pass filter 224; further, the paragraph at page 12, lines 17-19, discloses in part "an improved BTSC encoder that includes an input section, a sum channel processing section, and a difference channel processing section all of which are implemented using digital technology. Figure 8A shows that an encoded digital difference signal is produced by the difference channel processing section block 230; Figure 8B depicts "a difference channel processing section 230" block; Figure 3 and the paragraph at page 18, lines 16-26, state "the difference channel processing section 230 receives the difference signal and generates therefrom the encoded difference signal. The difference signal is applied to a low pass filter 238a which generates therefrom an output

signal that is applied to a fixed preemphasis filter 232a. The latter generates an output signal that is applied via line 239 to an input terminal of a wideband compression unit 280, and the encoded difference signal is applied via feedback line 240 to a detector terminal of wideband compression unit 280. The latter generates an output signal that is applied via line 281 to an input terminal of a spectral compression unit 290, and the encoded difference signal is also applied via feedback line 240 to a detector terminal of unit 290. The latter generates an output signal that is applied to a fixed preemphasis filter 232b which in turn generates an output signal that is applied to a clipper 254. Clipper 254 generates an output signal that is applied to a low pass filter 238b which in turn generates the encoded difference signal."

modulating the digital BTSC signal so as to produce a digital composite modulated BTSC signal.

As shown in Figure 9, and described on page 38, lines 21-23, "[f]igure 9 shows a block diagram of one embodiment of composite modulator 822. The latter receives the signals S and D and generates therefrom a digital version of the composite signal."

Claim 163

Independent claim 163 recites a circuit for encoding digital left and digital right audio signals according to the BTSC standard, comprising:

The paragraph at page 37, lines 21-22, and page 38, lines 3-4, of the specification describes, in reference to Figure 8B, "one preferred embodiment of a BTSC encoder 200b constructed according to the invention" which produces a "digital version of the composite signal"; and Figure 8B depicts the encoder 200b.

a digital matrix unit configured to generate a digital sum channel signal and a digital difference channel signal;

The paragraph at page 37, line 23, states that encoder 200b is similar to encoder 200a of Figure 8A; input section 210 of Figure 8B functions as a matrix as it receives L and R signals and produces sum (L+R) and difference (L-R) signals; the Abstract makes this clear "a matrix means for receiving the digital left and digital right filtered signals, and including means for

summing the digital left and digital right filtered signals and thereby generating a digital sum signal, and including means for subtracting one of the digital left and digital right filtered signals from the other of the digital left and digital right filtered signals and thereby generating a digital difference signal."

a sum channel processing unit; and

The paragraph at page 37, line 23, states that encoder 200b is similar to encoder 200a of Figure 8A; Figure 8A shows that a conditioned sum signal is produced by the sum channel processing section block 220, which is a digital component and equivalent to a sum channel processing unit; Figure 8B depicts "a sum channel processing section 220" block.

a difference channel processing unit;

The paragraph at page 37, line 23, states that encoder 200b is similar to encoder 200a of Figure 8A; Figure 8A shows that an encoded digital difference signal is produced by the difference channel processing section block 230, which is a digital component and equivalent to a difference channel processing unit; Figure 8B depicts "a difference channel processing section 230" block.

wherein said sum channel processing unit is configured to produce a conditioned digital sum channel signal in response to the digital sum channel signal, and the difference channel processing unit is configured to produce an encoded digital difference channel signal in response to the digital difference channel signal.

The paragraph at page 37, line 23, states that encoder 200b is similar to encoder 200a of Figure 8A; Figure 8A shows that a conditioned sum signal is produced by the sum channel processing section block 220, which is a digital component and equivalent to a digital sum channel section; Figure 8B depicts "a sum channel processing section 220" block; Figure 3 and the paragraph at page 16, lines 22-27, disclose that the sum channel processing section 220 includes a 75 μs preemphasis filter, a static phase equalization filter 228, and a low pass filter 224; further, the paragraph at page 12, lines 17-19, discloses in part "an improved BTSC encoder that includes an input section, a sum channel processing section, and a difference channel processing section all of which are implemented using digital technology. Figure 8A

shows that an encoded digital difference signal is produced by the difference channel processing section block 230; Figure 8B depicts "a difference channel processing section 230" block; Figure 3 and the paragraph at page 18, lines 16-26, state "the difference channel processing section 230 receives the difference signal and generates therefrom the encoded difference signal. The difference signal is applied to a low pass filter 238a which generates therefrom an output signal that is applied to a fixed preemphasis filter 232a. The latter generates an output signal that is applied via line 239 to an input terminal of a wideband compression unit 280, and the encoded difference signal is applied via feedback line 240 to a detector terminal of wideband compression unit 280. The latter generates an output signal that is applied via line 281 to an input terminal of a spectral compression unit 290, and the encoded difference signal is also applied via feedback line 240 to a detector terminal of unit 290. The latter generates an output signal that is applied to a fixed preemphasis filter 232b which in turn generates an output signal that is applied to a clipper 254. Clipper 254 generates an output signal that is applied to a low pass filter 238b which in turn generates the encoded difference signal."

Claim 166

Independent claim 166 recites a circuit for producing a digital composite modulated BTSC signal, comprising a matrix unit configured to produce a digital sum signal and a digital difference signal, a digital sum channel processing unit configured to produce a conditioned digital sum signal in response to the digital sum signal, and a digital difference channel processing unit conditioned to produce an encoded digital difference signal in response to the digital difference signal, and a digital modulator unit configured to produce a composite modulated signal in response to the encoded digital difference signal and the conditioned digital sum signal.

The paragraph at page 37, line 23, states that encoder 200b is similar to encoder 200a of Figure 8A; input section 210 of Figure 8B functions as a matrix as it receives L and R signals and produces sum (L+R) and difference (L-R) signals; the Abstract makes this clear "a matrix means for receiving the digital left and digital right filtered signals, and including means for summing the digital left and digital right filtered signals and thereby generating a digital sum

signal, and including means for subtracting one of the digital left and digital right filtered signals from the other of the digital left and digital right filtered signals and thereby generating a digital difference signal"; Figure 8A shows that a conditioned sum signal is produced by the sum channel processing section block 220, which is a digital component and equivalent to a sum channel processing unit; Figure 8B depicts a sum channel processing section 220 block; Figure 8A also shows that an encoded digital difference signal is produced by the difference channel processing section block 230, which is a digital component and equivalent to a difference channel processing unit; and Figure 8B depicts a difference channel processing section 230 block; Figures 8B and 9 show a composite modulator 822; the paragraph at page 38, lines 2-4, states in part that "encoder 200b includes a composite modulator 822 for receiving the signals S and D and for generating therefrom a digital version of the composite signal."

Claim 168

Independent claim 168 recites a digital signal processor comprising:

The paragraph at page 30, lines 11-12 and 14-15, discloses that "encoder 200 is preferably implemented using a single digital signal processing chip" and the "DSP Embodiment".

(a) an input section configured to receive one or more digital signals and derive therefrom a digital sum signal and a digital difference signal;

The paragraph at page 37, line 23, states that encoder 200b is similar to encoder 200a of Figure 8A; the paragraph at page 36, lines 10-11, explains that input section 210 of Figure 8A receives the L and R channels "and generates therefrom the sum signal that is applied to the sum channel processing section"; while the paragraph at page 36, lines 19-20, explains that "[i]nput section 210 also generates the difference signal that is applied to the difference channel processing section 230"; in a similar way, input section 210 of Figure 8B functions as a signal generator arrangement or matrix as it receives L and R signals and generates sum (L+R) and difference (L-R) signals.

(b) a digital difference channel section comprising (i) an adaptive signal weighting system configured to dynamically vary the amplitude and phase of the digital difference signal, and (ii) a frequency shifting system configured to alter the frequency of the digital difference signal according to the BTSC standard to produce a modified digital difference signal;

The paragraph at page 37, line 23, states that encoder 200b is similar to encoder 200a of Figure 8A; Figure 8A shows that an encoded digital difference signal is produced by the difference channel processing section block 230; Figure 8B depicts "a difference channel processing section 230" block; Figure 3 and the paragraph from page 18, line 16 to page 19, line 2, disclose that the difference channel processing section 230 includes a low pass filter 238a, a fixed preemphasis filter 232a, a wideband compression unit 280, spectral compression unit 290, fixed preemphasis filter 232b, clipper 254, and low pass filter 238b; further, the paragraph at page 12, lines 17-19, discloses in part "an improved BTSC encoder that includes an input section, a sum channel processing section, and a difference channel processing section all of which are implemented using digital technology."

(c) a digital sum channel section comprising one or more digital filters for altering the amplitude and phase of the digital sum signal according to the BTSC standard so as to produce a modified digital sum signal, and

The paragraph at page 37, line 23, states that encoder 200b is similar to encoder 200a of Figure 8A; Figure 8A shows that a conditioned sum signal is produced by the sum channel processing section block 220, which is a digital component and equivalent to a digital sum channel section; Figure 8B depicts "a sum channel processing section 220" block; Figure 3 and the paragraph at page 16, lines 22-27, disclose that the sum channel processing section 220 includes a 75 μs preemphasis filter, a static phase equalization filter 228, and a low pass filter 224; further, the paragraph at page 12, lines 17-19, discloses in part "an improved BTSC encoder that includes an input section, a sum channel processing section, and a difference channel processing section all of which are implemented using digital technology."

(d) an output section configured to combine the modified digital difference signal and modified digital sum signal and subsequently form one or more digital output signals.

Figures 8B and 9 show a composite modulator 822; the paragraph at page 38, lines 2-4, states in part that "encoder 200b includes a composite modulator 822 for receiving the signals S and D and for generating therefrom a digital version of the composite signal"; additionally, the paragraph at page 12, lines 10-12, discloses "a digital BTSC encoder including a composite modulator for generating a composite modulated signal from the conditioned sum signal and the encoded difference signal" [Emphasis added].

Claim 170

Independent claim 170 recites a digital signal processor comprising:

The paragraph at page 30, lines 11-12 and 14-15, discloses that "encoder 200 is preferably implemented using a single digital signal processing chip".

(a) an input section configured to receive one or more digital signals and derive therefrom a digital sum signal and digital difference signal;

The paragraph at page 37, line 23, states that encoder 200b is similar to encoder 200a of Figure 8A; the paragraph at page 36, lines 10-11, explains that input section 210 of Figure 8A receives the L and R channels "and generates therefrom the sum signal that is applied to the sum channel processing section"; while the paragraph at page 36, lines 19-20, explains that "[i]nput section 210 also generates the difference signal that is applied to the difference channel processing section 230"; in a similar way, input section 210 of Figure 8B functions as a signal generator arrangement or matrix as it receives L and R signals and generates sum (L+R) and difference (L-R) signals.

(b) a digital difference channel section comprising (i) an adaptive signal weighting system configured to dynamically vary the amplitude and phase of the digital difference signal, and (ii) a multiplier system configured to alter the frequency of the digital difference signal according to the BTSC standard to produce a modified digital difference signal;

The paragraph at page 37, line 23, states that encoder 200b is similar to encoder 200a of Figure 8A; Figure 8A shows that an encoded digital difference signal is produced by the difference channel processing section block 230; Figure 8B depicts "a difference channel

processing section 230" block; Figure 3 and the paragraph at page 18, lines 16-26, and page 19, lines 1-2, disclose that the difference channel processing section 230 includes a low pass filter 238a, a fixed preemphasis filter 232a, a wideband compression unit 280, spectral compression unit 290, fixed preemphasis filter 232b, clipper 254, and low pass filter 238b; further, the paragraph at page 12, lines 17-19, discloses in part "an improved BTSC encoder that includes an input section, a sum channel processing section, and a difference channel processing section all of which are implemented using digital technology."

(c) a digital sum channel section comprising one or more digital filters for altering the frequency and phase of said digital sum signal according to the BTSC standard to produce a modified digital sum signal; and

The paragraph at page 37, line 23, states that encoder 200b is similar to encoder 200a of Figure 8A; Figure 8A shows that a conditioned sum signal is produced by the sum channel processing section block 220, which is a digital component and equivalent to a digital sum channel section; Figure 8B depicts "a sum channel processing section 220" block; Figure 3 and the paragraph at page 16, lines 22-27, disclose that the sum channel processing section 220 includes a 75 μs preemphasis filter, a static phase equalization filter 228, and a low pass filter 224; further the paragraph at page 12, lines 17-19, discloses in part "an improved BTSC encoder that includes an input section, a sum channel processing section, and a difference channel processing section all of which are implemented using digital technology."

(d) an output section for combining said modified digital difference signal and modified digital sum signal to form one or more digital output signals.

Figures 8B and 9 show a composite modulator 822; the paragraph at page 38, lines 2-4, states in part that "encoder 200b includes a composite modulator 822 for receiving the signals S and D and for generating therefrom a digital version of the composite signal"; additionally, the paragraph at page 12, lines 10-12, discloses "a digital BTSC encoder including a composite modulator for generating a composite modulated signal from the conditioned sum signal and the encoded difference signal" [Emphasis added]).

Claim 171

Independent claim 171 recites a method of generating digital audio signals according to the BTSC standard comprising:

The paragraph at page 35, lines 6-7, of the specification describes, in reference to Figure 8A, "Figure 8A shows a block diagram that illustrates one method of using the DSP embodiment . . . "

a) accepting one or more digital audio input signals,

The paragraph at page 35, lines 9-11, of the specification describes, in reference to Figure 8A, "left and right channel audio input signals (shown in Figure 8A as 'L' and 'R,' respectively) and these signals are applied to the inputs of sixteen bit analog-to-digital converters 810 and 812, respectively."

b) performing a frequency translation of at least one digital audio signal to form at least one modified digital audio signal, and

The paragraph at page 41, lines 10-19, of the specification discloses in relation to Figure 8D "[p]ortion 822a includes two interpolators 910, 912, two low pass filters 914, 916, digital signal multiplier 918 and a digital signal adder 930. The S signal generated by module 296 is applied to interpolator 910 which 'up-samples' the S signal and applies the up-sampled signal to low pass filter 914. The latter filters this signal and applies the filtered signal to one input terminal of adder 930. A digital pilot tone having twice the normal amplitude (i.e., $2A\cos 2\pi(f_H/f_s)n$) is applied to the other input terminal of adder 930 which generates an output signal by summing the two signals present at its input terminals. The D signal generated by difference channel processing section 230 is applied to interpolator 912 which generates an up-sampled signal that is applied to low pass filter 916."

c) modifying the amplitude and phase of at least one of the digital audio signals according to the BTSC standard so as to create one or more corresponding digital audio output signals according to such standard.

The paragraph at page 12, lines 17-19, states in part "[t]hese and other objects are provided by an improved BTSC encoder that includes an input section, a sum channel processing

section, and a difference channel processing section, all of which are implemented using digital technology"; the paragraph at page 14, lines 17-20, states in part that "[f]igure 3 is a block diagram of one embodiment of a digital BTSC encoder 200 constructed according to the invention. Digital encoder 200 is constructed to provide performance that is functionally equivalent to the performance of idealized encoder 100 (shown in Figure 1)" [Emphasis added].

Claim 173

Independent claim 173 recites a digital signal processor comprising:

As shown in Figure 3, and discussed on page 14, lines 17-23, "[f]igure 3 is a block diagram of one embodiment of a digital BTSC encoder 200 constructed according to the invention.

a) an input section configured to receive one or more digital input signals;

The paragraph at page 35, lines 9-11, of the specification describes, in reference to Figure 8A, "left and right channel audio input signals (shown in Figure 8A as 'L' and 'R,' respectively) and these signals are applied to the inputs of sixteen bit analog-to-digital converters 810 and 812, respectively."

b) a sum-channel processing section for creating and conditioning a sum-channel signal according to the BTSC standard from the digital input signals;

The paragraph at page 37, line 23, states that encoder 200b is similar to encoder 200a of Figure 8A; Figure 8A shows that a conditioned sum signal is produced by the sum channel processing section block 220, which is a digital component and equivalent to a digital sum channel section; Figure 8B depicts "a sum channel processing section 220" block; Figure 3 and the paragraph at page 16, lines 22-27, disclose that the sum channel processing section 220 includes a 75 μs preemphasis filter, a static phase equalization filter 228, and a low pass filter 224; further, the paragraph at page 12, lines 17-19, discloses in part "an improved BTSC encoder that includes an input section, a sum channel processing section, and a difference channel processing section all of which are implemented using digital technology".

c) a difference-channel processing section for creating and filtering a difference-channel signal according to the BTSC standard from said digital input signals; and

Encoder 200 of Figure 3 includes a difference channel processing unit that includes seven filter blocks: low pass filter 238a, fixed preemphasis filter 232a, wideband compression unit 280, spectral compression unit 290, fixed preemphasis filter 232b, clipper 254, and low pass filter 238b; Figures 8A-8D and Figure 10 also show difference channel processing units; these portions of the specification provide support for "filtering a digital signal including difference-channel information so as to create a digital difference-channel signal".

d) a combining section for transforming the sum-channel signal and the difference-channel signal into one or more output signals according to the BTSC standard.

Figures 8B-8C and 9 show that the digital sum-channel signal and the digital difference channel signal are combined to form one or more digital output signals; in reference to Figure 8B, the paragraph at page 38, lines 2-4, states in part "encoder 200b includes a composite modulator 822 for receiving the signals S and D and for generating therefrom a digital version of the composite signal"; in reference to Figure 8C, the paragraph at page 40, lines 8-9, states in part "[c]omposite modulator 822 therefore generates from these signals a version of the composite signal"; in reference to Figure 9, the paragraph at page 39, lines 14-15, states in part ". . . signal adder 922 which generates the digital composite signal by summing the two signals present at its inputs"; thus these noted portions of the specification provide support for the limitation of "combining the sum-channel signal and the difference-channel signal so as to form one or more digital output signals"; the paragraph at page 14, lines 17-20, states in part that "[f]igure 3 is a block diagram of one embodiment of a digital BTSC encoder 200 constructed according to the invention. Digital encoder 200 is constructed to provide performance that is functionally equivalent to the performance of idealized encoder 100 (shown in Figure 1)" [Emphasis added].

Claim 174

Independent claim 174 recites a method of generating one or more digital output signals according to the BTSC standard, comprising:

The paragraph at page 35, lines 6-7, of the specification describes, in reference to Figure 8A, "[f]igure 8A shows a block diagram that illustrates one method of using the DSP embodiment . . . ."

filtering a digital signal including sum-channel information so as to create a digital sum-channel signal according to the BTSC standard,

Figure 3 shows a sum channel processing section 220 for a digital encoder according to the invention. See the paragraph from page 14, line 17, to page 15, line 6. Sum channel processing section 220 includes three filters in Figure 3: a 75 μs preemphasis filter 222, a static phase equalization filter 228, and a low pass filter 224; these portions of the specification support the limitation of "filtering a digital signal including sum-channel information so as to create a digital sum-channel signal" the paragraph at page 12, lines 17-19, states in part "[t]hese and other objects are provided by an improved BTSC encoder that includes an input section, a sum channel processing section, and a difference channel processing section, all of which are implemented using digital technology"; the paragraph at page 14, lines 17-20, states in part that "[f]igure 3 is a block diagram of one embodiment of a digital BTSC encoder 200 constructed according to the invention. Digital encoder 200 is constructed to provide performance that is functionally equivalent to the performance of idealized encoder 100 (shown in Figure 1)" [Emphasis added].

filtering a digital signal including difference-channel information so as to create a difference-channel signal according to the BTSC standard; and

Encoder 200 of Figure 3 includes a difference channel processing unit that includes seven filter blocks: low pass filter 238a, fixed preemphasis filter 232a, wideband compression unit 280, spectral compression unit 290, fixed preemphasis filter 232b, clipper 254, and low pass filter 238b; Figures 8A-8D and Figure 10 also show difference channel processing units; these portions of the specification provide support for "filtering a digital signal including difference-

channel information so as to create a digital difference-channel signal"; the paragraph at page 12, lines 17-19, states in part "[t]hese and other objects are provided by an improved BTSC encoder that includes an input section, a sum channel processing section, and a difference channel processing section, all of which are implemented using digital technology"; the paragraph at page 14, lines 17-20, states in part that "[f]igure 3 is a block diagram of one embodiment of a digital BTSC encoder 200 constructed according to the invention. Digital encoder 200 is constructed to provide performance that is functionally equivalent to the performance of idealized encoder 100 (shown in Figure 1)" [Emphasis added].

combining the sum-channel signal and the difference-channel signal so as to form one or more digital output signals according to the BTSC standard.

Figures 8B-8C and 9 show that the digital sum-channel signal and the digital difference channel signal are combined to form one or more digital output signals; in reference to Figure 8B, the paragraph at page 38, lines 2-4, states in part "encoder 200b includes a composite modulator 822 for receiving the signals S and D and for generating therefrom a digital version of the composite signal"; in reference to Figure 8C, the paragraph at page 40, lines 8-9, states in part "[c]omposite modulator 822 therefore generates from these signals a version of the composite signal"; in reference to Figure 9, the paragraph at page 39, lines 14-15, states in part ". . . signal adder 922 which generates the digital composite signal by summing the two signals present at its inputs".

Claim 176

Independent claim 176 recites a system for generating a broadcast television stereo signal from a left-channel signal and a right-channel signal, comprising:

As shown in Figure 3, and discussed on page 14, lines 17-23, "[f]igure 3 is a block diagram of one embodiment of a digital BTSC encoder 200 constructed according to the invention. Digital encoder 200 is constructed to provide performance that is functionally equivalent to the performance of idealized encoder 100 (shown in Figure 1). As with idealized encoder 100, digital encoder 200 receives the left and right channel audio input signals and

generates therefrom the conditioned sum signal and the encoded difference signal, however, in digital encoder 200 these input and output signals are digitally sampled signals rather than continuous analog signals."

a signal combiner arrangement configured so as to generate a summation signal comprising the sum of a right digital signal and a left digital signal, and generate a difference signal comprising the difference between the right digital signal and the left digital signal;

As shown in Figure 3, and described on page 16, lines 1-4, "[a]dder 216 generates a sum signal (indicated in Figure 3 as 'L+R') by summing the output signals generated by filters 212 and 214. Adder 218 generates a difference signal (indicated in Figure 3 as 'L-R') by subtracting the output signal generated by filter 214 from the output signal generated by filter 212."

a sum and difference signal generator arrangement configured so as to generate a first pre-emphasized digital signal as a function of the summation signal, and a second pre-emphasized digital signal as a function of the difference signal;

Sum channel processing section 220 with 75 μs preemphasis filter is shown in Figure 3 and described in the specification at page 16, lines 22-25, "[r]eferring again to Figure 3, the sum channel processing section 220 receives the sum signal and generates therefrom the conditioned sum signal. In particular, the sum signal is applied to a 75 μs preemphasis filter 222." Difference channel processing section 230 with fixed preemphasis filter 232a and fixed preemphasis filter 232b is shown in Figure 3 and described in the specification at page 18, line 16-26, as follows, "[r]eferring again to Figure 3, the difference channel processing section 230 receives the difference signal and generates therefrom the encoded difference signal. The difference signal is applied to a low pass filter 238a which generates therefrom an output signal that is applied to a fixed preemphasis filter 232a. The latter generates an output signal that is applied via line 239 to an input terminal of a wideband compression unit 280, and the encoded difference signal is applied via feedback line 240 to a detector terminal of wideband compression unit 280. The latter generates an output signal that is applied via line 281 to an input terminal of a spectral compression unit 290, and the encoded difference signal is also applied via feedback line 240 to a detector terminal of unit 290. The latter generates an output

signal that is applied to a fixed preemphasis filter 232b which in turn generates an output signal that is applied to a clipper 254."

a signal transformation arrangement configured so as to transform the first pre-emphasized digital signal to a digital BTSC compliant L+R signal, and transform the second pre-emphasized digital signal to a digital BTSC compliant L-R signal; and

Sum channel processing section 220 is described at page 16, lines 22-23, as follows, "[r]eferring again to Figure 3, the sum channel processing section 220 receives the sum signal and generates therefrom the conditioned sum signal." Difference channel processing section 230 is shown in Figure 3 and described at page 18, lines 16-17, as follows, "[r]eferring again to Figure 3, the difference channel processing section 230 receives the difference signal and generates therefrom the encoded difference signal." Sum channel processing section 220 and difference channel processing section 230 are also shown in Figure 8A.

a composite signal generator arrangement configured so as to generate a digital composite signal as a function of the combination of the digital BTSC compliant L+R signal and a modulated version of the digital BTSC compliant L-R signal.

Figures 8B-8C and 9 show that the digital sum-channel signal and the digital difference channel signal are combined to form one or more digital output signals; in reference to Figure 8B, the paragraph at page 38, lines 2-4, states in part "encoder 200b includes a composite modulator 822 for receiving the signals S and D and for generating therefrom a digital version of the composite signal"; in reference to Figure 8C, the paragraph at page 40, lines 8-9, states in part "[c]omposite modulator 822 therefore generates from these signals a version of the composite signal".

Claim 177

Independent claim 177 recites a method of generating a broadcast television stereo signal from a left-channel signal and a right-channel signal, comprising:

As shown in Figure 8A and described in the specification at page 35, lines 6-7, "[f]igure 8A shows a block diagram that illustrates one method of using the DSP Embodiment in an

analog system . . ." and at page 35, lines 8-10, "[t]he analog system supplies analog left and right channel audio input signals (shown in Figure 8A as 'L' and 'R', respectively) . . . ."

generating a summation signal comprising the sum of a right digital signal and a left digital signal, and generating a difference signal comprising the difference between the right digital signal and the left digital signal;

As shown in Figure 3, and described on page 15, line 23 through page 16, line 7, "[t]he input section 210 of encoder 200 includes two high pass filters 212, 214, and two signal adders 216, 218. The left channel digital audio input signal L is applied to the input of high pass filter 212, the latter generating therefrom an output signal that is applied to positive input terminals of adders 216, 218. The right channel audio input signal R is applied to the input of high pass filter 214 which generates therefrom an output signal that is applied to a positive input terminal of adder 216 and to a negative input terminal of adder 218. Adder 216 generates a sum signal (indicated in Figure 3 as 'L+R') by summing the output signals generated by filters 212 and 214. Adder 218 generates a difference signal (indicated in Figure 3 as 'L-R') by subtracting the output signal generated by filter 214 from the output signal generated by filter 212. Input section 210 is therefore similar to input section 110 (shown in Figure 1) however, section 210 additionally includes the two high pass filters 212, 214 and generates digital sum and difference signals."

generating a first pre-emphasized digital signal as a function of the summation signal, and generating a second pre-emphasized digital signal as a function of the difference signal;

As shown in Figure 3 for 75 μs preemphasis filter 222, fixed preemphasis filter 232a, and fixed preemphasis filter 232b and described on page 16, lines 22-27, "[r]eferring again to Figure 3, the sum channel processing section 220 receives the sum signal and generates therefrom the conditioned sum signal. In particular, the sum signal is applied to a 75 μs preemphasis filter 222. The filter 222 in turn generates an output signal that is applied to a static phase equalization filter 228. The filter 228 generates an output signal that is applied to a low pass filter 224 of section 220 which in turn generates the conditioned sum signal." And, again, at page 18, lines 16-26, "[r]eferring again to Figure 3, the difference channel processing section

230 receives the difference signal and generates therefrom the encoded difference signal. The difference signal is applied to a low pass filter 238a which generates therefrom an output signal that is applied to a fixed preemphasis filter 232a. The latter generates an output signal that is applied via line 239 to an input terminal of a wideband compression unit 280, and the encoded difference signal is applied via feedback line 240 to a detector terminal of wideband compression unit 280. The latter generates an output signal that is applied via line 281 to an input terminal of a spectral compression unit 290, and the encoded difference signal is also applied via feedback line 240 to a detector terminal of unit 290. The latter generates an output signal that is applied to a fixed preemphasis filter 232b which in turn generates an output signal that is applied to a clipper 254."

transforming the first pre-emphasized digital signal to a digital BTSC compliant L+R signal and transforming the second pre-emphasized digital signal to a digital BTSC compliant L-R signal;

Sum channel processing section 220 is shown in Figure 3 and described at page 16, lines 22-23, "[r]eferring again to Figure 3, the sum channel processing section 220 receives the sum signal and generates therefrom the conditioned sum signal." Difference channel processing section 230 is shown in Figure 3 and described at page 18, lines 16-17, "[r]eferring again to Figure 3, the difference channel processing section 230 receives the difference signal and generates therefrom the encoded difference signal." Sum channel processing section 220 and difference channel processing section 230 are also shown in Figure 8A.

generating a digital composite signal as a function of a combination of the digital BTSC compliant L+R signal and a modulated version of the digital BTSC compliant L-R signal.

As shown in Figure 9, and described on page 38, lines 21-23, "[f]igure 9 shows a block diagram of one embodiment of composite modulator 822. The latter receives the signals S and D and generates therefrom a digital version of the composite signal."

Claim 178

Independent claim 178 recites a system for generating a broadcast television stereo signal from a left digital signal and a right digital signal, comprising:

As shown in Figure 8A and described in the specification at page 35, lines 6-7, "[f]igure 8A shows a block diagram that illustrates one method of using the DSP Embodiment in an analog system . . ." and at page 35, lines 8-10, "[t]he analog system supplies analog left and right channel audio input signals (shown in Figure 8A as 'L' and 'R', respectively) . . . ."

(a) circuitry that generates a summation signal comprising the sum of the right digital signal and the left digital signal, and a difference signal comprising the difference between the right digital signal and the left digital signal;

As shown in Figure 3, and described on page 15, line 23 through page 16, line 7, "[t]he input section 210 of encoder 200 includes two high pass filters 212, 214, and two signal adders 216, 218. The left channel digital audio input signal L is applied to the input of high pass filter 212, the latter generating therefrom an output signal that is applied to positive input terminals of adders 216, 218. The right channel audio input signal R is applied to the input of high pass filter 214 which generates therefrom an output signal that is applied to a positive input terminal of adder 216 and to a negative input terminal of adder 218. Adder 216 generates a sum signal (indicated in Figure 3 as 'L+R') by summing the output signals generated by filters 212 and 214. Adder 218 generates a difference signal (indicated in Figure 3 as 'L-R') by subtracting the output signal generated by filter 214 from the output signal generated by filter 212. Input section 210 is therefore similar to input section 110 (shown in Figure 1) however, section 210 additionally includes the two high pass filters 212, 214 and generates digital sum and difference signals."

(b) preemphasis circuitry that generates a first digitally pre-emphasized signal corresponding to the summation signal, and a second digitally pre-emphasized signal corresponding to the difference signal; and

Sum channel processing section 220 with 75 μs preemphasis filter is shown in Figure 3 and described in the specification at page 16, lines 22-25, "[r]eferring again to Figure 3, the

sum channel processing section 220 receives the sum signal and generates therefrom the conditioned sum signal. In particular, the sum signal is applied to a 75 μs preemphasis filter 222." Difference channel processing section 230 with fixed preemphasis filter 232a and fixed preemphasis filter 232b is shown in Figure 3 and described in the specification at page 18, line 16-26, as follows, "[r]eferring again to Figure 3, the difference channel processing section 230 receives the difference signal and generates therefrom the encoded difference signal. The difference signal is applied to a low pass filter 238a which generates therefrom an output signal that is applied to a fixed preemphasis filter 232a. The latter generates an output signal that is applied via line 239 to an input terminal of a wideband compression unit 280, and the encoded difference signal is applied via feedback line 240 to a detector terminal of wideband compression unit 280. The latter generates an output signal that is applied via line 281 to an input terminal of a spectral compression unit 290, and the encoded difference signal is also applied via feedback line 240 to a detector terminal of unit 290. The latter generates an output signal that is applied to a fixed preemphasis filter 232b which in turn generates an output signal that is applied to a clipper 254."

(c) transforming circuitry that transforms the first pre-emphasized signal to a digital BTSC L+R signal and that transforms the pre-emphasized second signal to a digital BTSC L-R signal.

Sum channel processing section 220 is described at page 16, lines 22-23, as follows, "[r]eferring again to Figure 3, the sum channel processing section 220 receives the sum signal and generates therefrom the conditioned sum signal." Difference channel processing section 230 is shown in Figure 3 and described at page 18, lines 16-17, as follows, "[r]eferring again to Figure 3, the difference channel processing section 230 receives the difference signal and generates therefrom the encoded difference signal." Sum channel processing section 220 and difference channel processing section 230 are also shown in Figure 8A.

B. Identification of Means/Step Plus Function

No means plus function or step plus function limitations are recited in the claims on appeal.

Grounds of Rejection To Be Reviewed On Appeal

I. Claims 69-71, 78-87, 89-93, 106, 109, 110, 115, 117, 119, 134-174 and 176-184 ("Group A" claims) stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 4,760,602 to Gibson *et al.* ("Gibson") in view of appellant's admitted prior art ("AAPA") described in the Background section and shown in FIG. 1 of the subject application.

II. Claims 60-68, 72-77, 88, and 112-114 ("Group B" claims) stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Gibson in view of the AAPA, and in further view of Crochiere *et al.* ("Crochiere") ("Interpolation and Decimation of Digital Signals – A Tutorial Review").

Argument

I. Appellant's Group A Claims are not obvious under 35 U.S.C. § 103(a)

Claims 69-71, 78-87, 89-93, 106, 109, 110, 115, 117, 119, 134-174 and 176-184 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 4,760,602 to Gibson *et al.* ("Gibson") in view of appellant's admitted prior art ("AAPA") described in the Background section and shown in FIG. 1 of the subject application.

As a preliminary remark, appellant submits that the Examiner has disregarded certain limitations in the claims at issue, including those specifying that the claimed invention has digital components and operates digitally. Instead, the Examiner has treated such limitations as being merely functional language equivalent to an intended use. As required by MPEP § 2143.03, "[a]ll words in a claim must be considered in judging the patentability of that claim against the prior art," citing *In re Wilson*, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970). The Advisory Action issued 17 January 2012 illustrates the Examiner's treatment of such limitations:

> Appellant's claimed invention *has not specified any structure that is different from the combination of [the cited prior art].* Appellant has stated that many intended function [sic] of the disclosed invention, however, such intended function is not a part of the claimed invention.

As is explained below, the applied prior art does not teach or suggest the subject matter of appellant's claims, and thus the rejections under 35 U.S.C. § 103(a) should be reversed. The following remarks support the appellant's traverse of the rejections under 35 U.S.C. § 103(a).

Failure to Disclose or Suggest All Claim Limitations

Appellant respectfully submits that the prior art applied for the rejection of the Group A claims under 35 U.S.C. § 103(a) fails to disclose or suggest all the limitations of appellant's respective claims.

For all of the rejections of both the Group A and Group B claims under 35 U.S.C. § 103(a), the Examiner relies on Gibson as the primary reference. Gibson discloses an analog variable preemphasis/deemphasis network for providing compression/expansion in a second audio program (SAP) or stereophonic television (L-R) signal channel for noise reduction. Gibson, col. 1, lines 5-9. Figures 1A-1B of Gibson noted by the Examiner for the rejections do not show any digital architecture but rather show only *a prior art analog spectral compressor and expande*r respectively. See, Gibson, col. 2, lines 49-55.

One sentence of the Gibson disclosure is central to the rejections of the Group A and Group B claims. This one sentence, out of the entire Gibson disclosure, states that some of the Gibson implementations may be implemented in digital form. There is no teaching present in Gibson concerning enablement of such implementations, *i.e.*, how such implementations are to be practiced All embodiments shown and described in Gibson, in contrast, are *analog* embodiments. There is no teaching in Gibson about enabling *digital* BTSC compliant technology such as claimed by appellant. The particular portion of Gibson cited by the Examiner as allegedly disclosing "digital forms" actually states only the following:

> The illustrated embodiments *are implemented in continuous analog function*. Such a filter could be implemented in either continuous or sampled data form. *Sampled data implementations may be implemented in either analog or digital form.*
>
> [Emphasis added] (Gibson, col. 8, lines 11-16.)

As an example of the Examiner's logic, the following is provided for the rejection of appellant's independent claim 86:

> Gibson discloses a BTSC processor for L-R signal at the transmitter (shown in Figure 1A; col. 2, lines 56-60; col. 1, lines 52-54) and a BTSC processor at the receiver (shown in Figure 1B). *The adaptive weighting circuit could be implemented in analog or digital form (col. 8, lines 11-16)*. Thus, Gibson meets the claimed limitation as specified in B.
>
> [Emphasis Added]

Appellant submits that even though Gibson makes the conclusory statement (noted above) that implementations according to its disclosure may be implemented in digital form, *Gibson does not enable such digital implementations or describe a single digital embodiment with any specificity*. For enablement, it is not enough to simply state that something may be done. Underscoring this, *reductio ad absurdum*, the statement by itself that a cold fusion machine may be implemented, does not enable a cold fusion machine. Gibson (whether considered alone or in combination with the AAPA) does not disclose sufficient detail to enable a person of ordinary skill in the art to carry out appellant's claimed invention, *e.g.*, as recited in claim 86.

Continuing with the discussion of claim 86, the Examiner further states the following:

> Gibson fails to show the processor for L+R signal at the transmitter. However, BTSC encoder at the transmitter inherently includes processor for processing L+R signal. See col. 3, line 1 of Gibson. AAPA is cited here to clearly illustrate a processor for processing L+R signal and another processor for processing L-R signal. As illustrated in AAPA, the processor for processing L+R signal is simpler than the processor for processing L-R signal (see also in the background, p. 5, line 3+ of the instant application). *By using digital circuit for implementing a digital processor for processing L-R signal (with more complex design*

> *involved) as suggested in Gibson, one skilled in the art could expect that a digital processor could be designed for processing L+R signal (with less complex design comparing with processing L-R) without undue experience* [sic].
>
> [Emphasis added](Office Action, pages 3-4)

As was noted by the appellant previously, *Gibson discloses only analog embodiments of its spectral compressor and expanders, which operate (as the Examiner concedes) on only the L-R signal*. Gibson's sole comment that "[s]ampled data implementations may be implemented in either analog or digital form" does not enable one skilled in the art to achieve appellant's claimed invention; *the AAPA teaches only an analog BTSC-compliant system and does not remedy the deficiencies of Gibson*, as is explained below.

The AAPA, including Figure 1 and related text of the subject application, discloses a purely analog BTSC encoder system. The AAPA does not teach or suggest a digital BTSC encoder as recited in each of the claims under rejection. While the AAPA mentions that a digital BTSC encoder would potentially offer several advantages, the AAPA itself does not teach or suggest a digital BTSC encoder architecture as claimed by appellant , *e.g.*, in claim 86. To the contrary, the AAPA *clearly states that many difficulties were present for digital technology at the time of the invention of the claimed subject matter*, which is presumed to be when the original parent application was filed (*i.e.*, 07 June 1996); these difficulties are described by the AAPA as impeding development of a digital BTSC encoder:

> While a digital BTSC encoder would potentially offer several advantages, there is no simple way to construct an encoder using digital technology that is functionally equivalent to the idealized encoder 100 defined by the BTSC standard. One problem is that the BTSC standard defines all the critical components of idealized encoder 100 in terms of analog filter transfer functions. As is well known, while it is generally possible to design a digital filter so that either the magnitude or the phase response of the digital filter matches that of an analog filter, *it is extremely difficult to match both the amplitude and phase responses without requiring large amounts of processing capacity for processing*

data sampled at very high sampling rates or without significantly increasing the complexity of the digital filter. Without increasing either the sampling frequency or the filter order, the amplitude response of a digital filter can normally only be made to more closely match that of an analog filter at the expense of increasing the disparity between the phase responses of the two filters, and vice versa. However, since small errors in either amplitude or phase decrease the amount of separation provided by BTSC encoders, it would be essential for a digital BTSC encoder to closely match both the amplitude and phase responses of an idealized encoder of the type shown at 100 in Figure 1.

For a digital BTSC encoder to provide acceptable performance, it is critical to preserve the characteristics of the analog filters of an idealized encoder 100. Various techniques exist for designing a digital filter to match the performance of an analog filter; *however, in general, none of these techniques produce a digital filter (of the same order as the analog filter) having amplitude and phase responses that exactly match the corresponding responses of the analog filter*. Ideal encoder 100 is defined in terms of analog transfer functions specified in the frequency domain, or the s-plane, and to design a digital BTSC encoder, these transfer functions must be transformed to the z-plane. Such a transformation may be performed as a "many-to-one" mapping from the s-plane to the z-plane which attempts to preserve time domain characteristics. However, in such a transformation the frequency domain responses are subject to aliasing and may be altered significantly. Alternatively, the transformation may be performed as a "one-to-one" mapping from the s-plane to the z-plane that compresses the entire s-plane into the unit circle of the z-plane. However, *such a compression suffers from the familiar "frequency warping" between the analog and digital frequencies. Prewarping can be employed to compensate for this frequency warping effect, however, prewarping does not completely eliminate the deviations from the desired frequency response.* These problems would have to be overcome to produce a digital BTSC encoder that performs well and is not unduly complex or expensive.

(Appellant's specification at p. 9, line 23 to p. 11, line 2)[Emphasis added]

Appellant also notes that the difficulties described by the AAPA are corroborated by statements in the Declaration of John Strawn Pursuant to 37 C.F.R. § 1.132, submitted for the subject application on 15 April 2009. See paragraph 25 (discussing the AAPA):

> I agree with statements made in the Patent Application specification that "*there is no simple way to construct an encoder using digital technology that is functionally equivalent to the idealized encoder 100 defined by the BTSC standard*. [p. 9 lines 23-25]
>
> [Emphasis added]

Further discussing claim 86, the Examiner stated for the rejection (see Office Action, page 4) that the limitation defined in part D of the claim is "a functional statement" and one that is "inherently met according to [sic] BTSC standard that complies by [sic] Gibson and AAPA." Appellant notes that claim 86 is directed to a digital signal processor that processes digital audio signals and includes sections recited in (A),(B), and (C). These sections are digital components, as further characterized by the noted limitations in part D. Part D of claim 86 recites "wherein the difference between the *digital sum signal* and the *digital difference signal*, for a given frequency and level, *conforms with the difference specified by the BTSC standard*."

The Examiner appears to have disregarded all of the limitations in claim 86 that the signal processor is a digital one, and asserts that the D limitation of claim 86 is met by Gibson and AAPA because both describe circuits/systems that comply with the BTSC standard. Appellant notes again that Gibson and the AAPA disclose only *analog* BTSC circuits/systems and that while Gibson offers a conclusory statement about digital forms of its filter (*i.e.*, "*Sampled data implementations may be implemented in either analog or digital form")*, the patent does not enable or describe with any specificity any actual digital embodiments. Combining the teachings of the cited art would thus not achieve or make obvious the subject matter of appellant's claims. Thus, in actuality, the "D" limitation of claim 86 is not disclosed or suggested by Gibson and/or the AAPA.

Assuming for the sake of argument that the AAPA and Gibson are combined as proposed for the rejection, such a combination would still fail to achieve appellant's claimed subject matter, *e.g.*, as recited in claim 86. The AAPA and Gibson do not disclose *any digital architecture* (there is only Gibson's sole comment that "[s]ampled data implementations may be implemented in either analog or digital form") and do not disclose any specific digital methods.

For the rejection of claims 87 and 115, the Examiner stated that, compared to claim 86, the claimed system further includes a digital composite modulator. The Examiner then states that Gibson teaches a modulator (col. 2, lines 65+). Following this, the Examiner states:

> As discussed in [sic] claim 86, the L+R signal and the L-R signal are digitally processed. L+R or the L-R signal is a digital composite signal. *So the modulator used for modulating the digital L+R signal and the digital L-R signal could read on the claimed digital composite modulator.*
>
> [Emphasis added]

In response, appellant reiterates the rebuttal statements provided previously in response to the rejection of claim 86 and further submits that the conclusion made for the rejection of claims 87 and 115 is based on hindsight analysis to an impermissible degree (as is explained in further detail below in Section B "Lack of Proper Motivation for the Rejection"), as *neither Gibson nor the AAPA disclose or enable any specific digital processing or architecture*.

For the rejection of claim 89, the Examiner stated for the rejection that the claim was similar to claim 86. In response, appellant reiterates the rebuttal statements provided previously in response to the rejection of claim 86.

For the rejection of claim 90, the Examiner admitted that Gibson and AAPA fail to show that the digital matrix unit, the difference channel processing unit, and the sum channel processing unit are included in a single integrated circuit. The Examiner alleges that it would have been obvious to one of ordinary skill in the art to modify the combination of Gibson and the AAPA to try placing the digital matrix unit, the difference channel processing unit, and the sum

channel processing unit in a single integrated circuit in order to reduce the cost of the system and make a smaller system. (Office Action, page 6).

In response, appellant reiterates the rebuttal statements provided previously in response to the rejection of claim 86 and further submits that the conclusion made for the rejection of claim 90 is based on hindsight analysis to an impermissible degree, *as neither Gibson nor the AAPA disclose or enable any specific digital processing or architecture*. One skilled in the art, appreciating both the AAPA and Gibson, would need to perform undue experimentation, before arriving at the appellant's claimed subject matter, *e.g.*, as recited in claim 90; the AAPA and Gibson simply offer no guidance on implementing any digital technology.

For the rejection of claim 91, the Examiner admitted that Gibson and AAPA fail to show that the digital matrix unit, the difference channel processing unit, and the sum channel processing unit are implemented by a DSP. The Examiner then states that Gibson suggest a general digital circuitry. The Examiner then took Official Notice "that using a DSP to perform the digital processing function is notoriously well known in the art," concluding that "it would have been obvious to one of ordinary skill in the art to further modify Gibson and AAPA by using well known DSP in order to program the DSP to perform the digitized encoding function." (Office Action, page 6) In response, appellant reiterates the rebuttal statements provided previously in response to the rejection of claim 86 and further submits that the conclusion made for the rejection of claim 91 is based on hindsight analysis to an impermissible degree, as neither Gibson nor the AAPA disclose or enable any specific digital processing or architecture.

For the rejection of claims 69, 70, 78, 79, 80, and 81, the Examiner admitted that Gibson fails to show a digital-to-analog converter arrangement. The Examiner then makes the following comments:

> *By digitally processing the L+R signal and the L-R signal, they are digitally encoded signals*. Gibson teaches a general modulator (col. 2, lines 65+). A general analog modulator or a general digital modulator is well known in the art. With a general analog modulator, the digitally processed L+R signal and the digitally processed L-R signal have to be converted to analog format in order to

> be transmitted by the analog modulator. That is, DACs are at the inputs of a general analog modulator. On the other hand, when using a digital modulator, a DAC at the output of the digital modulator, could be used to convert the modulated digital signal to [sic] analog signal. Examiner takes Official Notice that DAC is notoriously well known in the art. *Thus, it would have been obvious to one of ordinary skill in the art to further modify Gibson and AAPA by including well-known DAC in order to use the analog modulator to combine the digitally processed L+R signal and L-R signal, or using well-known DAC for converting the digitally modulated composite signal.*
>
> [Emphasis added]

In response, appellant reiterates the rebuttal statements provided previously in response to the rejection of claim 86 and further submits that the noted conclusion made for the rejection of claims 69, 70, 78, 79, 80, and 81 is based on hindsight analysis to an impermissible degree, as neither Gibson nor the AAPA disclose or enable any specific digital processing or architecture. Furthermore, appellant notes that each of claims 69, 70, 78, 79, 80, and 81 includes the limitations of "*wherein the difference between the summation signal and the difference signal, for a given frequency and level, conforms with the difference specified by the BTSC standard*" and the limitations that the summation signal and difference signal *are digital signals*. As was explained previously, neither Gibson nor the AAPA disclose or suggest such limitations.

For the rejection of claim 71, the Examiner stated that the claimed "pre-selected sample rate" is inherently included in a digital signal. In response, appellant reiterates the rebuttal statements provided previously in response to the rejection of claim 86.

For the rejection of claims 82, 83, and 85, the Examiner stated that the limitation specified in the claims had been discussed for claim 86. In response, appellant reiterates the rebuttal statements provided previously in response to the rejection of claim 86.

For the rejection of claim 84, the Examiner stated that the claimed 75 μs preemphasis is inherently included in the BTSC standard. In response, appellant reiterates the rebuttal statements provided previously in response to the rejection of claim 86.

For the rejection of claim 92, the Examiner admitted that "comparing with claim 87 discussed above, Gibson fails to show the matrix unit has a frequency response in the digital domain that is substantially equal to the analog frequency response specified by the BTSC standard." The Examiner then states "[t]he AAPA discloses a matrix unit," "[t]his matrix unit could easily be designed to generate a digital L+R signal and a L-R signal without undue experience," and *"[t]he frequency response of the of the digital matrix unit should be similar to the frequency response of the equivalent analog matrix in order to preserve the signal contents (sum and difference channels)*." [Emphasis added] (Office Action, pages 7-8) The Examiner then took Official Notice that "this feature is notoriously well know in the art" and stated "[b]y using such matrix unit, the digital L-R signal could be processed by the digital processing unit as suggest in Gibson." (Office Action, page 8)

In response, appellant traverses the Examiner's taking Official Notice and reiterates the rebuttal statements provided previously in response to the rejection of claim 86. Appellant further submits that the noted conclusion made for the rejection of claim 92 is based on hindsight analysis to an impermissible degree, as neither Gibson nor the AAPA disclose or enable any specific digital processing or architecture.

In addition, appellant notes that at the time of appellant's invention, *i.e.*, as of the filing date of 07 June 1996 of the original priority document, Appellant was aware of no technology (beyond the appellant's) that could provide a digital architecture (such as claimed by appellant, *e.g.*, in claim 92) *that was able to provide a frequency response in the digital domain that was compliant with the frequency response in the analog domain as specified by the analog BTSC standard*.

This is clearly described in the Background section of appellant's specification. See appellant's specification at p. 9, line 23 to p. 11, line 2. . Thus, the appellant respectfully submits that the Examiner has failed to keep the priority date of the subject application in mind when formulating the rejection of claim 92 as well as those for the other pending claims of the application.

For the rejection of claim 93, the Examiner stated that the claimed frequency is an inherent feature of a BTSC broadcasting signal. In response, appellant reiterates the rebuttal statements provided previously in response to the rejection of claim 86.

For the rejection of claims 106 and 117, the Examiner stated that the limitations of the claims are similar to those in claims 86 and 87 with the exception of the adaptive signal weighting system configured to dynamically vary the phase of the digital difference signal, and the digital sum channel section comprising one or more digital filters for altering the phase of the digital sum signal. The Examiner then states that "*Gibson hints that the adaptive network for processing the difference signal would inherently vary the phase* (col. 2, lines 12-18)." [Emphasis added]

In response, Appellant reiterates the rebuttal statements provided previously in response to the rejection of claim 86. Further, the appellant respectfully takes issue with this statement concerning Gibson. What the cited portion of Gibson actually discloses is the following:

> A major disadvantage of the circuit shown in the above article is that two signal filters, one with a transfer characteristic H(f) and the other with the complementary transfer characteristic, *i.e.* H^{-1} (f), must be implemented. *The two signal filters must be accurately matched to each other in terms of both amplitude and phase for the circuit to operate properly.*
>
> [Emphasis added]

The cited text of Gibson clearly does not "hint" or otherwise imply or state that an adaptive network processing the difference signal would inherently vary the phase. In fact, the transfer functions (or characteristics) described by Gibson in the cited text do not reference or rely on phase at all: they are functions dependent on a single variable, frequency. Further, the noted transfer functions are not described by Gibson as affecting phase in any way. Regarding phase, the cited text of Gibson discloses only that the two signal filters, one with a given transfer characteristic and the other with the inverse transfer characteristic, "must be accurately matched." Gibson, col. 2, lines 17-18.

For the rejection of claims 109 and 119, the Examiner stated that the limitations in the claims are similar to those in claims 86 and 87 with the exception that the digital signal processor has a frequency response in the digital domain that is substantially equal to the analog frequency response specified by the BTSC standard. In response, appellant reiterates the rebuttal statements provided previously in response to the rejection of claim 86.

For the rejection of claims 110, the Examiner stated only that it is similar to claim 109. In response, appellant reiterates the rebuttal statements provided previously in response to the rejection of claim 86.

For the rejection of claims 134-174 and 176-183, the Examiner stated that these claims are substantially in the same form as claims 60-93, 106, 109, 112-115, 117, and 119, which were addressed previously in the Office Action. In response, regarding claims 134-174 and 176-183, the appellant reiterates the rebuttal statements provided previously in response to the rejection of claims 60-93, 106, 109, 112-115, 117, and 119.

Accordingly, appellant respectfully submits that Gibson and the AAPA form an improper basis for a rejection of claims 60-93, 106, 109, 110, 112-115, 117, 119, 134-174 and 176-184 under 35 U.S.C. § 103(a). Appellant, therefore, requests reversal of the rejection of the Group A claims.

II. Appellant's Group B Claims are not obvious under 35 U.S.C. § 103(a)

Claims 60-68, 72-77, 88, and 112-114 ("Group B" claims) stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Gibson and the AAPA, as described previously, and in further view of previously cited Crochiere *et al.* ("Crochiere") ("Interpolation and Decimation of Digital Signals – A Tutorial Review").

Crochiere is a tutorial review of interpolation and decimation of digital signals. Without acceding to the Examiner's characterizations of Crochiere, the reference is not understood as remedying the previously noted deficiencies of Gibson and the AAPA with respect to appellant's rejected claims of Group A. It is submitted that if one skilled in the art studied appellant's statement regarding the AAPA and the disclosures of Gibson as well as the disclosure of

Crochiere, the combination lacks the suggestions and teachings on how to implement a digital BTSC compatible device *that processes digital signals in a way that is compliant with the BTSC standard, which is an analog standard*, as defined by appellant's Group B claims.

Applicant therefore requests reversal of the rejection of claims 60-68, 72-77, 88, and 112-114 under 35 U.S.C. § 103(a).

Conclusion

For all of the foregoing reason, Appellant respectfully submit that the rejections of the claims of the subject application are based on improper grounds and should be reversed. Appellant, therefore, respectfully solicits the Honorable Board to reverse the Examiner's rejections of the claims of the subject application under 35 U.S.C. § 103.

To the extent necessary, a petition for an extension of time under 37 CFR § 1.136 is hereby made. Please charge the fees for a Petition for Extension of Time under 37 CFR § 1.136, and any other required fees, to Deposit Account 501133.

Respectfully submitted,
McDERMOTT WILL & EMERY LLP

___/G. Matthew McCloskey/_____

G. Matthew McCloskey
Registration No. 47,025

28 State Street
Boston, MA 02109
Phone: 617.535.4082
Facsimile: 617.535.3800
Date: 30 July 2012

Please recognize our Customer No. 23630 as our correspondence address.

CLAIMS APPENDIX

60. A system for generating an analog broadcast television stereo signal from a left-channel signal and a right-channel signal, comprising:

an analog-to-digital converter arrangement configured so as to convert the right-channel signal to a right digital signal and convert the left-channel signal to a left digital signal;

a signal combiner arrangement coupled to the analog-to-digital converter arrangement and configured so as to generate a summation signal comprising the sum of the right digital signal and the left digital signal, and generate a difference signal comprising the difference between the right digital signal and the left digital signal;

a first up-sampler configured to insert additional samples into the summation signal to increase the sample rate of the summation signal;

a second up-sampler configured to insert additional samples into the difference signal to increase the sample rate of the difference signal;

a sum and difference signal generator arrangement configured so as to generate a first pre-emphasized digital signal as a function of the summation signal, and a second pre-emphasized digital signal as a function of the difference signal;

a signal transformation arrangement configured so as to transform the first pre-emphasized digital signal to a digital BTSC compliant L+R signal, and transform the second pre-emphasized digital signal to a digital BTSC compliant L-R signal;

a digital-to-analog converter arrangement configured to convert the digital BTSC compliant L+R signal to an analog BTSC compliant L+R signal, and the digital BTSC compliant L-R signal to an analog BTSC compliant L-R signal; and

a composite signal generator arrangement configured so as to generate a composite signal as a function of the combination of the analog BTSC compliant L+R signal and a modulated version of the analog BTSC compliant L-R signal.

61. The system according to claim 60, wherein the sum and difference signal generator arrangement comprises a digital signal processor arrangement programmed to digitally add pre-emphasis to each of the summation and difference signals.

62. The system according to claim 60, wherein the signal transformation arrangement comprises an L-R data path and an L+R data path, each path having a preselected sample rate.

63. A method of generating an analog broadcast television stereo signal from a left-channel signal and a right-channel signal, comprising:

converting the right-channel signal to a right digital signal and converting the left-channel signal to a left digital signal;

generating a summation signal comprising the sum of the right digital signal and the left digital signal, and generating a difference signal comprising the difference between the right digital signal and the left digital signal;

with a first up-sampler, inserting additional samples into the summation signal to increase the sample rate of the summation signal;

with a second up-sampler, inserting additional samples into the difference signal to increase the sample rate of the difference signal;

generating a first pre-emphasized digital signal as a function of the summation signal, and generating a second pre-emphasized digital signal as a function of the difference signal;

transforming the first pre-emphasized digital signal to a digital BTSC compliant L+R signal and transforming the second pre-emphasized digital signal to a digital BTSC compliant L-R signal;

converting the digital BTSC compliant L+R signal to an analog BTSC compliant L+R signal, and converting the digital BTSC compliant L-R signal to an analog BTSC compliant L-R signal; and

generating a composite signal as a function of a combination of the analog BTSC compliant L+R signal and a modulated version of the analog BTSC compliant L-R signal.

64. The method according to claim 63, further comprising:

generating a modulated version of the analog BTSC compliant L-R signal after converting the digital BTSC L-R signal to an analog BTSC compliant L-R signal.

65. The method according to claim 63, wherein the step of generating the first pre-emphasized digital signal and generating the second pre-emphasized digital signal comprises:

using a programmed digital signal processor arrangement to digitally add pre-emphasis to each of the summation and difference signals.

66. The method according to claim 63, wherein the step of transforming the first pre-emphasized signal and transforming the second pre-emphasized signal comprises:

sampling the first pre-emphasized signal at a first preselected sample rate, and sampling the second pre-emphasized signal at a second preselected sample rate.

67. A method of generating an analog broadcast television stereo signal from a left-channel signal and a right-channel signal, comprising:

converting the right-channel signal to a right digital signal;

converting the left-channel signal to a left digital signal;

generating a summation signal comprising the sum of the right digital signal and the left digital signal;

generating a difference signal comprising the difference between the right digital signal and the left digital signal;

with a first up-sampler, inserting additional samples into the summation signal to increase the sample rate of the summation signal;

with a second up-sampler, inserting additional samples into the difference signal to increase the sample rate of the difference signal;

generating a first pre-emphasized digital signal corresponding to the summation signal;

generating a second pre-emphasized digital signal corresponding to the difference signal;

transforming the first pre-emphasized digital signal to a digital BTSC compliant L+R signal;

transforming the second pre-emphasized digital signal to a digital BTSC compliant L-R signal;

converting the digital BTSC compliant L+R signal to an analog BTSC compliant L+R signal;

converting the digital BTSC compliant L-R signal to an analog BTSC compliant L-R signal; and

generating a composite signal as a function of a combination of the analog BTSC compliant L+R signal with a modulated version of the analog BTSC compliant L-R signal.

68. The method according to claim 67, further comprising:

generating a modulated version of the analog BTSC compliant L-R signal after converting the digital BTSC compliant L-R signal to an analog BTSC compliant L-R signal.

69. A system for generating an analog broadcast television stereo signal from a left-channel signal and a right-channel signal, comprising:

an analog-to-digital converter arrangement configured so as to convert the right-channel signal to a right digital signal and convert the left-channel signal to a left digital signal;

a signal combiner arrangement coupled to the analog-to-digital converter arrangement and configured so as to generate a summation signal comprising the sum of the right digital signal and the left digital signal, and generate a difference signal comprising the difference between the right digital signal and the left digital signal; wherein the difference between the summation signal and the difference signal, for a given frequency and level, conforms with the difference specified by the BTSC standard;

a sum and difference signal generator arrangement configured so as to generate a first pre-emphasized digital signal as a function of the summation signal, and a second pre-emphasized digital signal as a function of the difference signal;

a signal transformation arrangement configured so as to transform the first pre-emphasized digital signal to a digital BTSC compliant L+R signal, and transform the second pre-emphasized digital signal to a digital BTSC compliant L-R signal;

a composite signal generator arrangement configured so as to generate a digital composite signal as a function of the combination of the digital BTSC compliant L+R signal and a modulated version of the digital BTSC compliant L-R signal; and

a digital-to-analog converter arrangement configured to convert the digital composite signal to an analog composite signal.

70. (Previously Presented) The system according to claim 69, wherein the sum and difference signal generator arrangement comprises a digital signal processor arrangement programmed to digitally add pre-emphasis to each of the summation and difference signals.

71. (Previously Presented) The system according to claim 69, wherein the signal transformation arrangement comprises an L-R data path and an L+R data path, each path having a preselected sample rate.

72. (Previously Presented) A method of generating an analog broadcast television stereo signal from a left-channel signal and a right-channel signal, comprising:

converting the right-channel signal to a right digital signal and converting the left-channel signal to a left digital signal;

generating a summation signal comprising the sum of the right digital signal and the left digital signal, and generating a difference signal comprising the difference between the right digital signal and the left digital signal;

with a first up-sampler, inserting additional samples into the summation signal to increase the sample rate of the summation signal;

with a second up-sampler, inserting additional samples into the difference signal to increase the sample rate of the difference signal;

generating a first pre-emphasized digital signal as a function of the summation signal, and generating a second pre-emphasized digital signal as a function of the difference signal;

transforming the first pre-emphasized digital signal to a digital BTSC compliant L+R signal and transforming the second pre-emphasized digital signal to a digital BTSC compliant L-R signal;

generating a digital composite signal as a function of a combination of the digital BTSC compliant L+R signal and a modulated version of the digital BTSC compliant L-R signal; and

converting the digital composite signal to an analog composite signal.

73. The method according to claim 72, further comprising:

generating a modulated version of the digital BTSC compliant L-R signal before converting the digital composite signal to an analog composite signal.

74. The method according to claim 72, wherein generating the first pre-emphasized digital signal and generating the second pre-emphasized digital signal comprises:

using a programmed digital signal processor arrangement to digitally add pre-emphasis to each of the summation and difference signals.

75. The method according to claim 72, wherein transforming the first pre-emphasized digital signal and transforming the second pre-emphasized digital signal comprises:

sampling the first pre-emphasized digital signal at a first preselected sample rate, and sampling the second pre-emphasized digital signal at a second preselected sample rate.

76. A method of generating a broadcast television stereo signal from a left-channel signal and a right-channel signal, comprising:

converting the right-channel signal to a right digital signal;

converting the left-channel signal to a left digital signal;

generating a summation signal comprising the sum of the right digital signal and the left digital signal;

generating a difference signal comprising the difference between the right digital signal and the left digital signal;

with a first up-sampler, inserting additional samples into the summation signal to increase the sample rate of the summation signal;

with a second up-sampler, inserting additional samples into the difference signal to increase the sample rate of the difference signal;

generating a first pre-emphasized digital signal corresponding to the summation signal;

generating a second pre-emphasized digital signal corresponding to the difference signal;

transforming the first pre-emphasized digital signal to a digital BTSC compliant L+R signal;

transforming the second pre-emphasized digital signal to a digital BTSC compliant L-R signal;

generating a digital composite signal as a function of a combination of the digital BTSC compliant L+R signal with a modulated version of the digital BTSC compliant L-R signal; and

converting the digital composite signal to an analog composite signal.

77. The method according to claim 76, further comprising:

generating a modulated version of the digital BTSC compliant L-R signal before generating the digital composite signal.

78. A digital signal processor arrangement for use in generating a broadcast television BTSC encoded stereo signal from a left-channel signal and a right-channel signal, comprising:

a signal generator arrangement configured so as to generate a digital summation signal as a function of the sum of the left-channel and right-channel signals, and a digital difference signal as a function of the difference between the left-channel and right-channel signals; wherein the difference between the digital summation signal and the digital difference signal, for a given frequency and level, conforms with the difference specified by the BTSC standard;

a summation signal processing arrangement including a filter arrangement configured to filter the digital summation signal so as to produce a conditioned digital summation signal;

a difference signal processing arrangement including a pre-emphasis filter arrangement and a signal compressor arrangement, the filter and signal compressor arrangements being configured so as to condition and compress the digital difference signal so as to produce a conditioned digital difference signal;

a digital-to-analog converter arrangement for converting the conditioned digital summation signal to an analog sum signal, and the conditioned digital difference signal to an analog difference signal; and

a signal combiner arrangement configured so as to combine the analog sum signal with a modulated version of the analog difference signal.

79. An arrangement in accordance with claim 78, wherein the filter arrangement of the summation signal processing arrangement is configured so as to filter the digital summation signal with a 75μs pre-emphasis so as to produce a conditioned digital summation signal.

80. A digital signal processor arrangement for use in generating a broadcast television BTSC encoded stereo signal from a left-channel signal and a right-channel signal, comprising:

a signal generator arrangement configured so as to generate a digital summation signal as a function of the sum of the left-channel and right-channel signals, and a digital difference signal as a function of the difference between the left-channel and right-channel signals; wherein the difference between the digital summation signal and the digital difference signal, for a given frequency and level, conforms with the difference specified by the BTSC standard;

a summation signal processing arrangement including a filter arrangement configured to filter the digital summation signal so as to produce a conditioned digital summation signal;

a difference signal processing arrangement including a pre-emphasis filter arrangement and a signal compressor arrangement, the filter and compressor arrangements being configured so as to condition and compress the digital difference signal so as to produce a conditioned digital difference signal;

a signal combiner arrangement configured so as to combine the conditioned digital summation signal with a modulated version of the conditioned digital difference signal so as to generate a composite modulated signal; and

a digital-to-analog converter arrangement for converting the composite modulated signal to an analog output signal.

81. An arrangement in accordance with claim 80, wherein the filter arrangement of the summation signal processing arrangement is configured so as to filter the digital summation signal with a 75μs pre-emphasis so as to produce a conditioned digital summation signal.

82. A method of digitally encoding left and right channel audio signals in accordance with the BTSC standard, comprising:

providing digital left and digital right channel audio signals;

combining the digital left and digital right channel audio signals to form a digital sum signal and a digital difference signal, wherein the difference between the digital sum signal and the digital difference signal, for a given frequency and level, conforms with the difference specified by the BTSC standard; and

encoding the digital sum signal and the digital difference signal according to the BTSC standard so as to produce a digital BTSC signal.

83. A method of digitally encoding left and right channel audio signals according to claim 82, wherein providing digital left and digital right channel audio signals includes receiving analog left and right channel audio signals and digitizing the analog left and right channel audio signals so as to produce the digital left and right channel audio signals.

84. A method of digitally encoding left and right channel audio signals according to claim 82, wherein encoding the digital sum signal and the digital difference signal according to the BTSC standard includes encoding the digital sum channel with an applied 75μs preemphasis.

85. A method of digitally encoding left and right channel audio signals according to claim 82, wherein encoding the digital sum signal and the digital difference signal according to the BTSC standard includes encoding the digital difference signal with an adaptive signal weighting system.

86. A digital signal processor for producing a signal encoded according to the BTSC standard, said digital signal processor comprising:

A) an input section constructed and arranged so as to (1) receive digital left and digital right audio signals and (2) combine the digital left and digital right audio signals so as to form a digital sum signal and a digital difference signal;

B) a difference channel processing section constructed and arranged so as to encode the digital difference signal according to the BTSC standard; and

C) a sum channel processing section constructed and arranged so as to condition the digital sum signal according to the BTSC standard;

D) wherein the difference between the digital sum signal and the digital difference signal, for a given frequency and level, conforms with the difference specified by the BTSC standard.

87. A system for producing a digital composite modulated BTSC signal comprising a digital BTSC encoder arranged so as to generate a digital BTSC encoded signal, and a digital composite modulator, wherein the digital BTSC encoder comprises (i) a difference channel processing section constructed and arranged so as to encode a digital difference signal according to the BTSC standard, and (ii) a sum channel processing section constructed and arranged so as to condition a digital sum signal according to the BTSC standard; wherein the BTSC encoder has a frequency response in the digital domain that is substantially equal to the analog frequency response specified by the BTSC standard.

88. A method of generating a digital composite modulated BTSC signal, comprising:

generating digital left and digital right channel audio signals;

combining said digital left and digital right channel audio signals so as to form a digital sum signal and a digital difference signal;

with a first up-sampler, inserting additional samples into the digital sum signal to increase the sample rate of the digital sum signal;

with a second up-sampler, inserting additional samples into the digital difference signal to increase the sample rate of the digital difference signal;

encoding the digital sum signal and digital difference signal according to the BTSC standard so as to produce a digital BTSC signal; and

modulating the digital BTSC signal so as to produce a digital composite modulated BTSC signal.

89. A circuit for encoding digital left and digital right audio signals according to the BTSC standard, comprising:

a digital matrix unit configured to generate a digital sum channel signal and a digital difference channel signal;

a sum channel processing unit; and

a difference channel processing unit;

wherein said sum channel processing unit is configured to produce a conditioned digital sum channel signal in response to the digital sum channel signal, and the difference channel processing unit is configured to produce an encoded digital difference channel signal in response to the digital difference channel signal; and wherein the digital matrix has a frequency response in the digital domain that is substantially equal to the analog frequency response specified by the BTSC standard.

90. A circuit for encoding digital left and digital right audio signals according to claim 89, wherein the digital matrix unit, the difference channel processing unit, and the sum channel processing unit are included on a single integrated circuit.

91. A circuit for encoding digital left and digital right audio signals according to claim 89, wherein the digital matrix unit, the difference channel processing unit, and the sum channel processing unit are implemented by a digital signal processor.

92. A circuit for producing a digital composite modulated BTSC signal, comprising a matrix unit configured to produce a digital sum signal and a digital difference signal, a digital sum channel processing unit configured to produce a conditioned digital sum signal in response to the digital sum signal, and a digital difference channel processing unit conditioned to produce an encoded digital difference signal in response to the digital difference signal, and a digital modulator unit configured to produce a composite modulated signal in response to the encoded digital difference signal and the conditioned digital sum signal;

wherein the matrix unit has a frequency response in the digital domain that is substantially equal to the analog frequency response specified by the BTSC standard.

93. A circuit for producing a digital composite modulated BTSC signal according to claim 92, wherein the digital modulator unit is configured to modulate the encoded digital difference signal at a frequency substantially equal to 31,468 Hz.

106. A digital signal processor comprising

(a) an input section configured to receive one or more digital signals and derive therefrom a digital sum signal and digital difference signal;

(b) a digital difference channel section comprising (i) an adaptive signal weighting system configured to dynamically vary the amplitude and phase of the digital difference signal, and (ii) a multiplier system configured to alter the frequency of the digital difference signal according to the BTSC standard to produce a modified digital difference signal, wherein the adaptive signal weighting system is configured to vary the amplitude of substantially all the spectrum within the digital difference signal responsive to the amplitude of substantially all the spectrum within the digital difference signal;

(c) a digital sum channel section comprising one or more digital filters for altering the frequency and phase of said digital sum signal according to the BTSC standard to produce a modified digital sum signal; and

(d) an output section for combining said modified digital difference signal and modified digital sum signal to form one or more digital output signals.

109. A digital signal processor comprising

a) an input section configured to receive one or more digital input signals;

b) a sum-channel processing section for creating and conditioning a sum-channel signal according to the BTSC standard from the digital input signals

c) a difference-channel processing section for creating and filtering a difference-channel signal according to the BTSC standard from said digital input signals; and

d) a combining section for transforming the sum-channel signal and the difference-channel signal into one or more output signals according to the BTSC standard;

wherein the digital signal processor has a frequency response in the digital domain that is substantially equal to the analog frequency response specified by the BTSC standard.

110. A method of generating one or more digital output signals according to the BTSC standard, comprising:

filtering a digital signal including sum-channel information so as to create a digital sum-channel signal according to the BTSC standard;

filtering a digital signal including difference-channel information so as to create a digital difference-channel signal according to the BTSC standard; and

combining the sum-channel signal and the difference-channel signal so as to form one or more digital output signals according to the BTSC standard, wherein the difference between the sum-channel signal and the difference-channel signal, for a given frequency and level, conforms with the difference specified by the BTSC standard.

112. A system for generating a broadcast television stereo signal from a left-channel signal and a right-channel signal, comprising:

a signal combiner arrangement configured so as to generate a summation signal comprising the sum of a right digital signal and a left digital signal, and generate a difference signal comprising the difference between the right digital signal and the left digital signal;

a sum and difference signal generator arrangement configured so as to generate a first pre-emphasized digital signal as a function of the summation signal, and a second pre-emphasized digital signal as a function of the difference signal;

a signal transformation arrangement configured so as to transform the first pre-emphasized digital signal to a digital BTSC compliant L+R signal, and transform the second pre-emphasized digital signal to a digital BTSC compliant L-R signal, wherein the difference between the digital BTSC compliant L+R signal and the digital BTSC compliant L-R signal, for a given frequency and level, conforms with the difference specified by the BTSC standard; and

a composite signal generator arrangement configured so as to generate a digital composite signal as a function of the combination of the digital BTSC compliant L+R signal and a modulated version of the digital BTSC compliant L-R signal.

113. A method of generating a broadcast television stereo signal from a left-channel signal and a right-channel signal, comprising:

generating a summation signal comprising the sum of a right digital signal and a left digital signal, and generating a difference signal comprising the difference between the right digital signal and the left digital signal;

generating a first pre-emphasized digital signal as a function of the summation signal, and generating a second pre-emphasized digital signal as a function of the difference signal;

transforming the first pre-emphasized digital signal to a digital BTSC compliant L+R signal and transforming the second pre-emphasized digital signal to a digital BTSC compliant L-R signal, wherein the difference between the digital BTSC compliant L+R signal and the digital BTSC compliant L-R signal, for a given frequency and level, conforms with the difference specified by the BTSC standard; and

generating a digital composite signal as a function of a combination of the digital BTSC compliant L+R signal and a modulated version of the digital BTSC compliant L-R signal.

114. A system for generating a broadcast television stereo signal from a left digital signal and a right digital signal, comprising:

(a) circuitry that generates a summation signal comprising the sum of the right digital signal and the left digital signal, and a difference signal comprising the difference between the right digital signal and the left digital signal;

(b) preemphasis circuitry that generates a first digitally pre-emphasized signal corresponding to the summation signal, and a second digitally pre-emphasized signal corresponding to the difference signal; and

(c) transforming circuitry that transforms the first pre-emphasized signal to a digital BTSC L+R signal and that transforms the pre-emphasized second signal to a digital BTSC L-R signal; wherein the difference between the digital BTSC L+R signal and the digital BTSC L-R signal, for a given frequency and level, conforms with the difference specified by the BTSC standard.

115. A system for producing a digital composite modulated BTSC signal according to claim 87, wherein the digital composite modulator is arranged to generate the digital composite modulated BTSC signal responsively to and as a function of the BTSC encoded signal.

117. The digital signal processor according to claim 106, wherein the digital output signals are BTSC encoded digital output signals.

119. The digital signal processor according to claim 109, wherein the digital output signals are BTSC encoded output signals.

134. A system for generating a broadcast television stereo signal from a left-channel signal and a right-channel signal, comprising:

an analog-to-digital converter arrangement configured so as to convert the right-channel signal to a right digital signal and convert the left-channel signal to a left digital signal;

a signal combiner arrangement coupled to the analog-to-digital converter arrangement and configured so as to generate a summation signal comprising the sum of the right digital signal and the left digital signal, and generate a difference signal comprising the difference between the right digital signal and the left digital signal;

a sum and difference signal generator arrangement configured so as to generate a first pre-emphasized digital signal as a function of the summation signal, and a second pre-emphasized digital signal as a function of the difference signal;

a signal transformation arrangement configured so as to transform the first pre-emphasized digital signal to a digital BTSC compliant L+R signal, and transform the second pre-emphasized digital signal to a digital BTSC compliant L-R signal;

a digital-to-analog converter arrangement configured to convert the digital BTSC compliant L+R signal to an analog BTSC compliant L+R signal, and the digital BTSC compliant L-R signal to an analog BTSC compliant L-R signal; and

a composite signal generator arrangement configured so as to generate a composite signal as a function of the combination of the analog BTSC compliant L+R signal and a modulated version of the analog BTSC compliant L-R signal.

135. The system according to claim 134, wherein the sum and difference signal generator arrangement comprises a digital signal processor arrangement programmed to digitally add pre-emphasis to each of the summation and difference signals.

136. The system according to claim 134, wherein the signal transformation arrangement comprises an L-R data path and an L+R data path, each path having a preselected sample rate.

137. A method of generating a broadcast television stereo signal from a left-channel signal and a right-channel signal, comprising:

converting the right-channel signal to a right digital signal and converting the left-channel signal to a left digital signal;

generating a summation signal comprising the sum of the right digital signal and the left digital signal, and generating a difference signal comprising the difference between the right digital signal and the left digital signal;

generating a first pre-emphasized digital signal as a function of the summation signal, and generating a second pre-emphasized digital signal as a function of the difference signal;

transforming the first pre-emphasized digital signal to a digital BTSC compliant L+R signal and transforming the second pre-emphasized digital signal to a digital BTSC compliant L-R signal;

converting the digital BTSC compliant L+R signal to an analog BTSC compliant L+R signal, and converting the digital BTSC compliant L-R signal to an analog BTSC compliant L-R signal; and

generating a composite signal as a function of a combination of the analog BTSC compliant L+R signal and a modulated version of the analog BTSC compliant L-R signal.

138. The method according to claim 137, further comprising:

generating a modulated version of the analog BTSC compliant L-R signal after converting the digital BTSC L-R signal to an analog BTSC compliant L-R signal.

139. The method according to claim 137, wherein the step of generating the first pre-emphasized digital signal and generating the second pre-emphasized digital signal comprises:

using a programmed digital signal processor arrangement to digitally add pre-emphasis to each of the summation and difference signals.

140. The method according to claim 137, wherein the step of transforming the first pre-emphasized signal and transforming the second pre-emphasized signal comprises:

sampling the first pre-emphasized signal at a first preselected sample rate, and sampling the second pre-emphasized signal at a second preselected sample rate.

141. A method of generating a broadcast television stereo signal from a left-channel signal and a right-channel signal, the method comprising:

converting the right-channel signal to a right digital signal;

converting the left-channel signal to a left digital signal;

generating a summation signal comprising the sum of the right digital signal and the left digital signal;

generating a difference signal comprising the difference between the right digital signal and the left digital signal;

generating a first pre-emphasized digital signal corresponding to the summation signal;

generating a second pre-emphasized digital signal corresponding to the difference signal;

transforming the first pre-emphasized digital signal to a digital BTSC compliant L+R signal;

transforming the second pre-emphasized digital signal to a digital BTSC compliant L-R signal;

converting the digital BTSC compliant L+R signal to an analog BTSC compliant L+R signal;

converting the digital BTSC compliant L-R signal to an analog BTSC compliant L-R signal; and

generating a composite signal as a function of a combination of the analog BTSC compliant L+R signal with a modulated version of the analog BTSC compliant L-R signal.

142. (Previously Presented) The method according to claim 141, further comprising:

generating a modulated version of the analog BTSC compliant L-R signal after converting the digital BTSC compliant L-R signal to an analog BTSC compliant L-R signal.

143. A system for generating a broadcast television stereo signal from a left-channel signal and a right-channel signal, comprising:

an analog-to-digital converter arrangement configured so as to convert the right-channel signal to a right digital signal and convert the left-channel signal to a left digital signal;

a signal combiner arrangement coupled to the analog-to-digital converter arrangement and configured so as to generate a summation signal comprising the sum of the right digital signal and the left digital signal, and generate a difference signal comprising the difference between the right digital signal and the left digital signal;

a sum and difference signal generator arrangement configured so as to generate a first pre-emphasized digital signal as a function of the summation signal, and a second pre-emphasized digital signal as a function of the difference signal;

a signal transformation arrangement configured so as to transform the first pre-emphasized digital signal to a digital BTSC compliant L+R signal, and transform the second pre-emphasized digital signal to a digital BTSC compliant L-R signal;

a composite signal generator arrangement configured so as to generate a digital composite signal as a function of the combination of the digital BTSC compliant L+R signal and a modulated version of the digital BTSC compliant L-R signal; and

a digital-to-analog converter arrangement configured to convert the digital composite signal to an analog composite signal.

144. The system according to claim 143, wherein the sum and difference signal generator arrangement comprises a digital signal processor arrangement programmed to digitally add pre-emphasis to each of the summation and difference signals.

145. The system according to claim 143, wherein the signal transformation arrangement comprises an L-R data path and an L+R data path, each path having a preselected sample rate.

146. A method of generating a broadcast television stereo signal from a left-channel signal and a right-channel signal, comprising:

converting the right-channel signal to a right digital signal and converting the left-channel signal to a left digital signal;

generating a summation signal comprising the sum of the right digital signal and the left digital signal, and generating a difference signal comprising the difference between the right digital signal and the left digital signal;

generating a first pre-emphasized digital signal as a function of the summation signal, and generating a second pre-emphasized digital signal as a function of the difference signal;

transforming the first pre-emphasized digital signal to a digital BTSC compliant L+R signal and transforming the second pre-emphasized digital signal to a digital BTSC compliant L-R signal;

generating a digital composite signal as a function of a combination of the digital BTSC compliant L+R signal and a modulated version of the digital BTSC compliant L-R signal; and

converting the digital composite signal to an analog composite signal.

147. The method according to claim 146, further comprising:

generating a modulated version of the digital BTSC compliant L-R signal before converting the digital composite signal to an analog composite signal.

148. The method according to claim 146, wherein generating the first pre-emphasized digital signal and generating the second pre-emphasized digital signal comprises:

using a programmed digital signal processor arrangement to digitally add pre-emphasis to each of the summation and difference signals.

149. The method according to claim 146, wherein transforming the first pre-emphasized digital signal and transforming the second pre-emphasized digital signal comprises:

sampling the first pre-emphasized digital signal at a first preselected sample rate, and sampling the second pre-emphasized digital signal at a second preselected sample rate.

150. A method of generating a broadcast television stereo signal from a left-channel signal and a right-channel signal, the method comprising:

converting the right-channel signal to a right digital signal;

converting the left-channel signal to a left digital signal;

generating a summation signal comprising the sum of the right digital signal and the left digital signal;

generating a difference signal comprising the difference between the right digital signal and the left digital signal;

generating a first pre-emphasized digital signal corresponding to the summation signal;

generating a second pre-emphasized digital signal corresponding to the difference signal;

transforming the first pre-emphasized digital signal to a digital BTSC compliant L+R signal;

transforming the second pre-emphasized digital signal to a digital BTSC compliant L-R signal;

generating a digital composite signal as a function of a combination of the digital BTSC compliant L+R signal with a modulated version of the digital BTSC compliant L-R signal; and

converting the digital composite signal to an analog composite signal.

151. The method according to claim 150, further comprising:

generating a modulated version of the digital BTSC compliant L-R signal before generating the digital composite signal.

152. A digital signal processor arrangement for use in generating a broadcast television BTSC encoded stereo signal from a left-channel signal and a right-channel signal, comprising:

a signal generator arrangement configured so as to generate a digital summation signal as a function of the sum of the left-channel and right-channel signals, and a digital difference signal as a function of the difference between the left-channel and right-channel signals;

a summation signal processing arrangement including a filter arrangement configured to filter the digital summation signal so as to produce a conditioned digital summation signal;

a difference signal processing arrangement including a pre-emphasis filter arrangement and a signal compressor arrangement, the filter and signal compressor arrangements being configured so as to condition and compress the digital difference signal so as to produce a conditioned digital difference signal;

a digital-to-analog converter arrangement for converting the conditioned digital summation signal to an analog sum signal, and the conditioned digital difference signal to an analog difference signal; and

a signal combiner arrangement configured so as to combine the analog sum signal with a modulated version of the analog difference signal.

153. An arrangement in accordance with claim 152, wherein the filter arrangement of the summation signal processing arrangement is configured so as to filter the digital summation signal with a 75μs pre-emphasis so as to produce a conditioned digital summation signal.

154. A digital signal processor arrangement for use in generating a broadcast television BTSC encoded stereo signal from a left-channel signal and a right-channel signal, comprising:

a signal generator arrangement configured so as to generate a digital summation signal as a function of the sum of the left-channel and right-channel signals, and a digital difference signal as a function of the difference between the left-channel and right-channel signals;

a summation signal processing arrangement including a filter arrangement configured to filter the digital summation signal so as to produce a conditioned digital summation signal;

a difference signal processing arrangement including a pre-emphasis filter arrangement and a signal compressor arrangement, the filter and compressor arrangements being configured so as to condition and compress the digital difference signal so as to produce a conditioned digital difference signal;

a signal combiner arrangement configured so as to combine the conditioned digital summation signal with a modulated version of the conditioned digital difference signal so as to generate a composite modulated signal; and

a digital-to-analog converter arrangement for converting the composite modulated signal to an analog output signal.

155. An arrangement in accordance with claim 154, wherein the filter arrangement of the summation signal processing arrangement is configured so as to filter the digital summation signal with a 75μs pre-emphasis so as to produce a conditioned digital summation signal.

156. A method of digitally encoding left and right channel audio signals in accordance with the BTSC standard, comprising:

providing digital left and digital right channel audio signals;

combining the digital left and digital right channel audio signals to form a digital sum signal and a digital difference signal; and

encoding the digital sum signal and the digital difference signal according to the BTSC standard so as to produce a digital BTSC signal.

157. A method of digitally encoding left and right channel audio signals according to claim 156, wherein providing digital left and digital right channel audio signals includes receiving analog left and right channel audio signals and digitizing the analog left and right channel audio signals so as to produce the digital left and right channel audio signals.

158. A method of digitally encoding left and right channel audio signals according to claim 156, wherein encoding the digital sum signal and the digital difference signal according to the BTSC standard includes encoding the digital sum channel with an applied 75μs preemphasis.

159. A method of digitally encoding left and right channel audio signals according to claim 156, wherein encoding the digital sum signal and the digital difference signal according to

the BTSC standard includes encoding the digital difference signal with an adaptive signal weighting system.

160. A digital signal processor for producing a signal encoded according to the BTSC standard, said digital signal processor comprising:

A) an input section constructed and arranged so as to (1) receive digital left and digital right audio signals and (2) combine the digital left and digital right audio signals so as to form a digital sum signal and a digital difference signal;

B) a difference channel processing section constructed and arranged so as to encode the digital difference signal according to the BTSC standard; and

C) a sum channel processing section constructed and arranged so as to condition the digital sum signal according to the BTSC standard.

161. A system for producing a digital composite modulated BTSC signal comprising a digital BTSC encoder arranged so as to generate a digital BTSC encoded signal, and a digital composite modulator.

162. A method of generating a digital composite modulated BTSC signal, comprising:

generating digital left and digital right channel audio signals,

combining said digital left and digital right channel audio signals so as to form a digital sum signal and a digital difference signal,

encoding the digital sum signal and digital difference signal according to the BTSC standard so as to produce a digital BTSC signal, and

modulating the digital BTSC signal so as to produce a digital composite modulated BTSC signal.

163. A circuit for encoding digital left and digital right audio signals according to the BTSC standard, comprising:

a digital matrix unit configured to generate a digital sum channel signal and a digital difference channel signal;

a sum channel processing unit; and

a difference channel processing unit;

wherein said sum channel processing unit is configured to produce a conditioned digital sum channel signal in response to the digital sum channel signal, and the difference channel processing unit is configured to produce an encoded digital difference channel signal in response to the digital difference channel signal.

164. A circuit for encoding digital left and digital right audio signals according to claim 163, wherein the digital matrix unit, the difference channel processing unit, and the sum channel processing unit are included on a single integrated circuit.

165. A circuit for encoding digital left and digital right audio signals according to claim 163, wherein the digital matrix unit, the difference channel processing unit, and the sum channel processing unit are implemented by a digital signal processor.

166. A circuit for producing a digital composite modulated BTSC signal, comprising a matrix unit configured to produce a digital sum signal and a digital difference signal, a digital sum channel processing unit configured to produce a conditioned digital sum signal in response to the digital sum signal, and a digital difference channel processing unit conditioned to produce an encoded digital difference signal in response to the digital difference signal, and a digital modulator unit configured to produce a composite modulated signal in response to the encoded digital difference signal and the conditioned digital sum signal.

167. A circuit for producing a digital composite modulated BTSC signal according to claim 166, wherein the digital modulator unit is configured to modulate the encoded digital difference signal at a frequency substantially equal to 31,468 Hz.

168. A digital signal processor comprising:

(a) an input section configured to receive one or more digital signals and derive therefrom a digital sum signal and a digital difference signal;

(b) a digital difference channel section comprising (i) an adaptive signal weighting system configured to dynamically vary the amplitude and phase of the digital difference signal, and (ii) a frequency shifting system configured to alter the frequency of the digital difference signal according to the BTSC standard to produce a modified digital difference signal;

(c) a digital sum channel section comprising one or more digital filters for altering the amplitude and phase of the digital sum signal according to the BTSC standard so as to produce a modified digital sum signal, and

(d) an output section configured to combine the modified digital difference signal and modified digital sum signal and subsequently form one or more digital output signals.

169. A digital signal processor according to Claim 168, wherein said frequency shifting system is configured to alter the frequency of the digital difference signal by substantially 31.468 kHz.

170. A digital signal processor comprising

(a) an input section configured to receive one or more digital signals and derive therefrom a digital sum signal and digital difference signal;

(b) a digital difference channel section comprising (i) an adaptive signal weighting system configured to dynamically vary the amplitude and phase of the digital difference signal, and (ii) a multiplier system configured to alter the frequency of the digital difference signal according to the BTSC standard to produce a modified digital difference signal;

(c) a digital sum channel section comprising one or more digital filters for altering the frequency and phase of said digital sum signal according to the BTSC standard to produce a modified digital sum signal; and

(d) an output section for combining said modified digital difference signal and modified digital sum signal to form one or more digital output signals.

171. A method of generating digital audio signals according to the BTSC standard comprising:

a) accepting one or more digital audio input signals,

b) performing a frequency translation of at least one digital audio signal to form at least one modified digital audio signal, and

c) modifying the amplitude and phase of at least one of the digital audio signals according to the BTSC standard so as to create one or more corresponding digital audio output signals according to such standard.

172. A method of generating digital audio signals according to Claim 171, wherein performing the frequency translation of the least one digital audio signal includes performing the frequency translation by substantially 31.468 kHz.

173. A digital signal processor comprising:

a) an input section configured to receive one or more digital input signals;

b) a sum-channel processing section for creating and conditioning a sum-channel signal according to the BTSC standard from the digital input signals;

c) a difference-channel processing section for creating and filtering a difference-channel signal according to the BTSC standard from said digital input signals; and

d) a combining section for transforming the sum-channel signal and the difference-channel signal into one or more output signals according to the BTSC standard.

174. A method of generating one or more digital output signals according to the BTSC standard, comprising:

filtering a digital signal including sum-channel information so as to create a digital sum-channel signal according to the BTSC standard,

filtering a digital signal including difference-channel information so as to create a difference-channel signal according to the BTSC standard; and

combining the sum-channel signal and the difference-channel signal so as to form one or more digital output signals according to the BTSC standard.

176. A system for generating a broadcast television stereo signal from a left-channel signal and a right-channel signal, comprising:

a signal combiner arrangement configured so as to generate a summation signal comprising the sum of a right digital signal and a left digital signal, and generate a difference signal comprising the difference between the right digital signal and the left digital signal;

a sum and difference signal generator arrangement configured so as to generate a first pre-emphasized digital signal as a function of the summation signal, and a second pre-emphasized digital signal as a function of the difference signal;

a signal transformation arrangement configured so as to transform the first pre-emphasized digital signal to a digital BTSC compliant L+R signal, and transform the second pre-emphasized digital signal to a digital BTSC compliant L-R signal; and

a composite signal generator arrangement configured so as to generate a digital composite signal as a function of the combination of the digital BTSC compliant L+R signal and a modulated version of the digital BTSC compliant L-R signal.

177. A method of generating a broadcast television stereo signal from a left-channel signal and a right-channel signal, comprising:

generating a summation signal comprising the sum of a right digital signal and a left digital signal, and generating a difference signal comprising the difference between the right digital signal and the left digital signal;

generating a first pre-emphasized digital signal as a function of the summation signal, and generating a second pre-emphasized digital signal as a function of the difference signal;

transforming the first pre-emphasized digital signal to a digital BTSC compliant L+R signal and transforming the second pre-emphasized digital signal to a digital BTSC compliant L-R signal;

generating a digital composite signal as a function of a combination of the digital BTSC compliant L+R signal and a modulated version of the digital BTSC compliant L-R signal.

178. A system for generating a broadcast television stereo signal from a left digital signal and a right digital signal, comprising:

(a) circuitry that generates a summation signal comprising the sum of the right digital signal and the left digital signal, and a difference signal comprising the difference between the right digital signal and the left digital signal;

(b) preemphasis circuitry that generates a first digitally pre-emphasized signal corresponding to the summation signal, and a second digitally pre-emphasized signal corresponding to the difference signal; and

(c) transforming circuitry that transforms the first pre-emphasized signal to a digital BTSC L+R signal and that transforms the pre-emphasized second signal to a digital BTSC L-R signal.

179. A system for producing a digital composite modulated BTSC signal according to claim 161, wherein the digital composite modulator is arranged to generate the digital composite modulated BTSC signal responsively to and as a function of the BTSC encode signal.

180. The digital signal processor according to claim 168, wherein the digital output signals are encoded in accordance with the BTSC standard.

181. The digital signal processor according to claim 170, wherein the digital output signals are BTSC encoded digital output signals.

182. The method according to claim 171, wherein the digital audio output signal is a BTSC encoded digital audio output signal.

183. The digital signal processor according to claim 173, wherein the digital output signals are BTSC encoded output signals.

EVIDENCE APPENDIX

Declaration of John Strawn Pursuant to 37 C.F.R. § 1.132, submitted for the subject application on 15 April 2009.

RELATED PROCEEDINGS APPENDIX

None.